SIITME 2026
IEEE 32nd International Symposium for
Design and Technology in Electronics Packaging
28th - 31st October 2026, Târgoviște, Romania
Conference & Exhibition



Keynote speaker:

Name: Cătălin Ciobanu
Job position: Associate Professor
***Company:* Transilvania University of Brasov**
Job position: Senior Researcher
***Company:* National Institute for Research and Development in Microtechnologies - IMT Bucharest**

e-mail: catalin.ciobanu@unitbv.ro
catalin.ciobanu@imt.ro

Title of the Presentation:
ISOLDE: Building Blocks for High-Performance RISC-V Systems

Short CV

Cătălin Ciobanu has a MSc and PhD from Delft University of Technology, The Netherlands. He is currently Associate Professor at Transilvania University of Brasov, Romania and Senior Researcher at the National Institute for Research and Development in Microtechnologies - IMT Bucharest, Romania. His research interests include RISC-V processors, embedded systems, high-performance computing, SIMD architectures, digital signal processing and reconfigurable hardware.

Abstract

The pursuit for technological sovereignty is a cornerstone of the European industrial strategy. A key element in this endeavor is the availability of high-performance yet still energy-efficient computing resources. To prevent long-term vendor lock-in and reduce critical dependence on proprietary Intellectual Property (IP), the European Union is pivoting towards open-source solutions. A transparent, flexible, and strong ecosystem around RISC-V is essential, and key European actors from academia and industry are working together to create a unified hardware-software design environment that enables customization and optimization for various application classes. Fully in line with these European strategic goals is the Chips Joint Undertaking (Chips-JU)-funded project ISOLDE (High Performance, Safe, Secure, Open-Source Leveraged RISC-V Domain-Specific Ecosystems). Launched in 2023, ISOLDE expands this hardware ecosystem to the application level. It targets the delivery of industrial-grade open-source hardware and software for complex SoCs. This includes a focus on high-performance superscalar and 64-bit cores with out-of-order execution (centered around CVA6 and NOEL-V) as well as specialized hardware accelerators.