Enabling Advanced Chiplet and SiP Architectures: Materials, Interconnects, and Thermal Solutions.

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Speaker:

Martin Metzler, Director Technical Business Development Europe

MacDermid Alpha ELECTRONICS SOLUTIONS

Martin Metzler

Director, Technical Business Development
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My journey through the KEYNOTE presentation and the preparation

The finalization of the pictures took 10 runs, with several adaptations on my and the background.

Standard GPU: NVIDIA A100; GPU-time: 30-60sec; Compute-capacity: 3-12PFLOP*s; Energy: ~2Wh

Evolution in the data center sector:

V100 (Volta) = 0,4 A100 (Ampere) = baseline H100 (Hopper) = 3x H200 (Hopper+) = 4x

2017 **2020** **2022** **2024**

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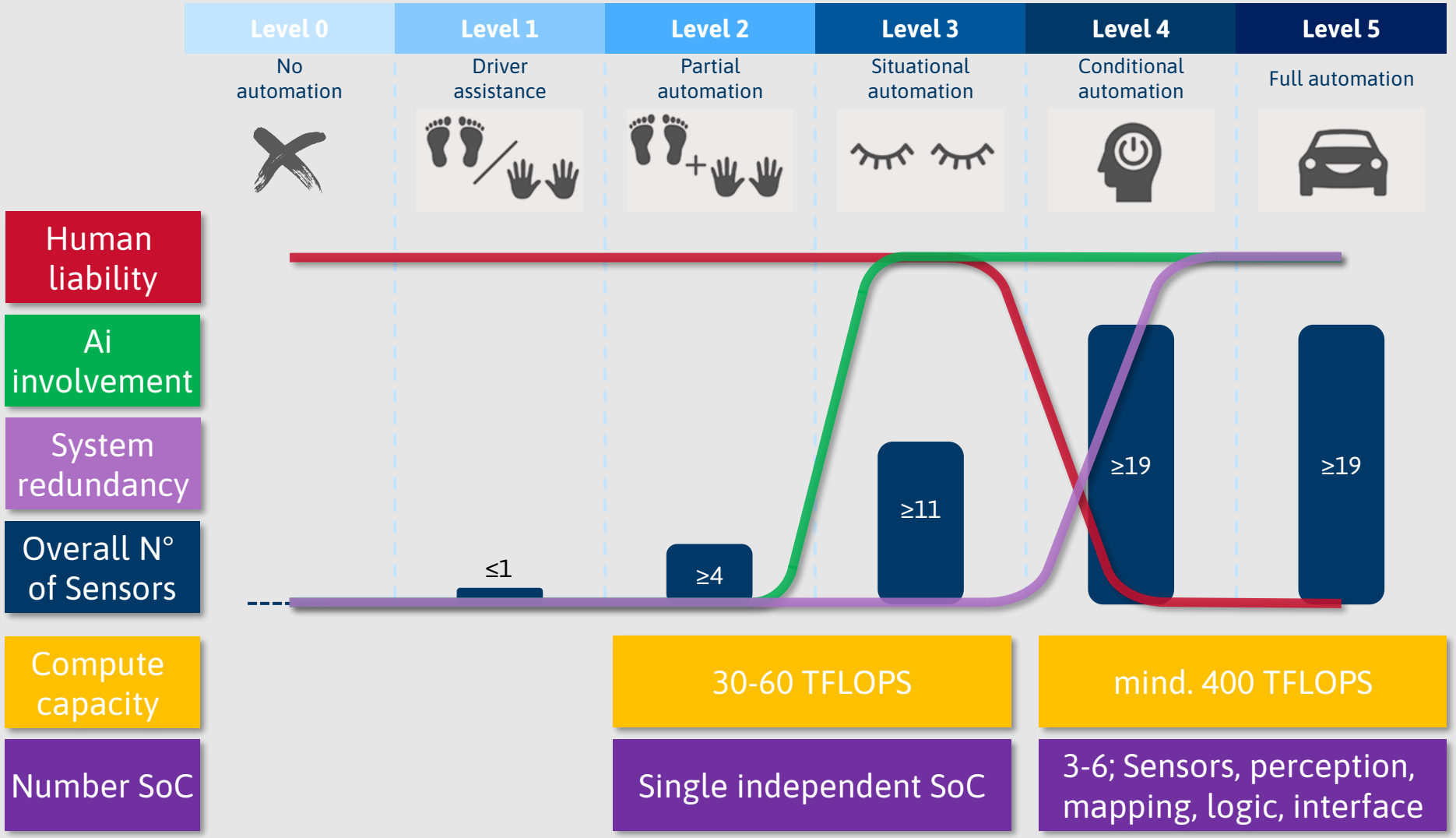
Market Trend in Autonomous Driving

ADAS Levels (SAE J3016), Source: IDTechEX; Cloud factory and market assumption



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Advanced Packaging:

- **2.5D Integration** of Dies
  - Side-by-side integration of multiple Dies
  - High-Density interconnects, Micro-Bumps
  - Silicon, Organic or Glas interposer
  - Through-Silicone-Vias (TSV) on Silicon Interposer
  - EMIB, Embedded Multi-DieInterconnectBridge (Intel)
- **3D Integration** of Dies
  - Vertical integration, stacking of multiple Dies
  - TSV Stacking with hybrid bonding
- **Fan-Out Packaging** like FO-WLP or FO-PLP
  - Redistribution Layers (RDL) without a classical substrate
- **System-in-Packages (SiP)** as functional, final system
  - Combination of Dies, passive Components, MEMS and Sensors
- **Embedded** Die and Substrate integration
- **Hybrid Packages** as combination of 2.5D + 3D + SiP

Drivers for Advanced Packaging:

- **Cost Efficiency**
  - Higher yield in Die production
  - Multiple usage of Chiplets
- **Higher Performance**
  - Shorter signal paths
  - Higher signal integrity
  - Lower latency
- **Higher Energy Density** and **Efficiency**
- **Improved Thermal management**, high power/ energy densities can be controlled
- **Application-Specific** use of customized and **optimized Technology** (heterogeneous integration)

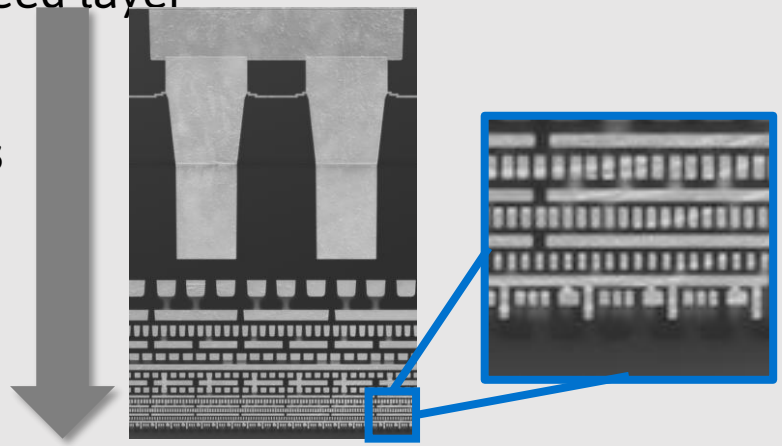
Interconnect Technologies

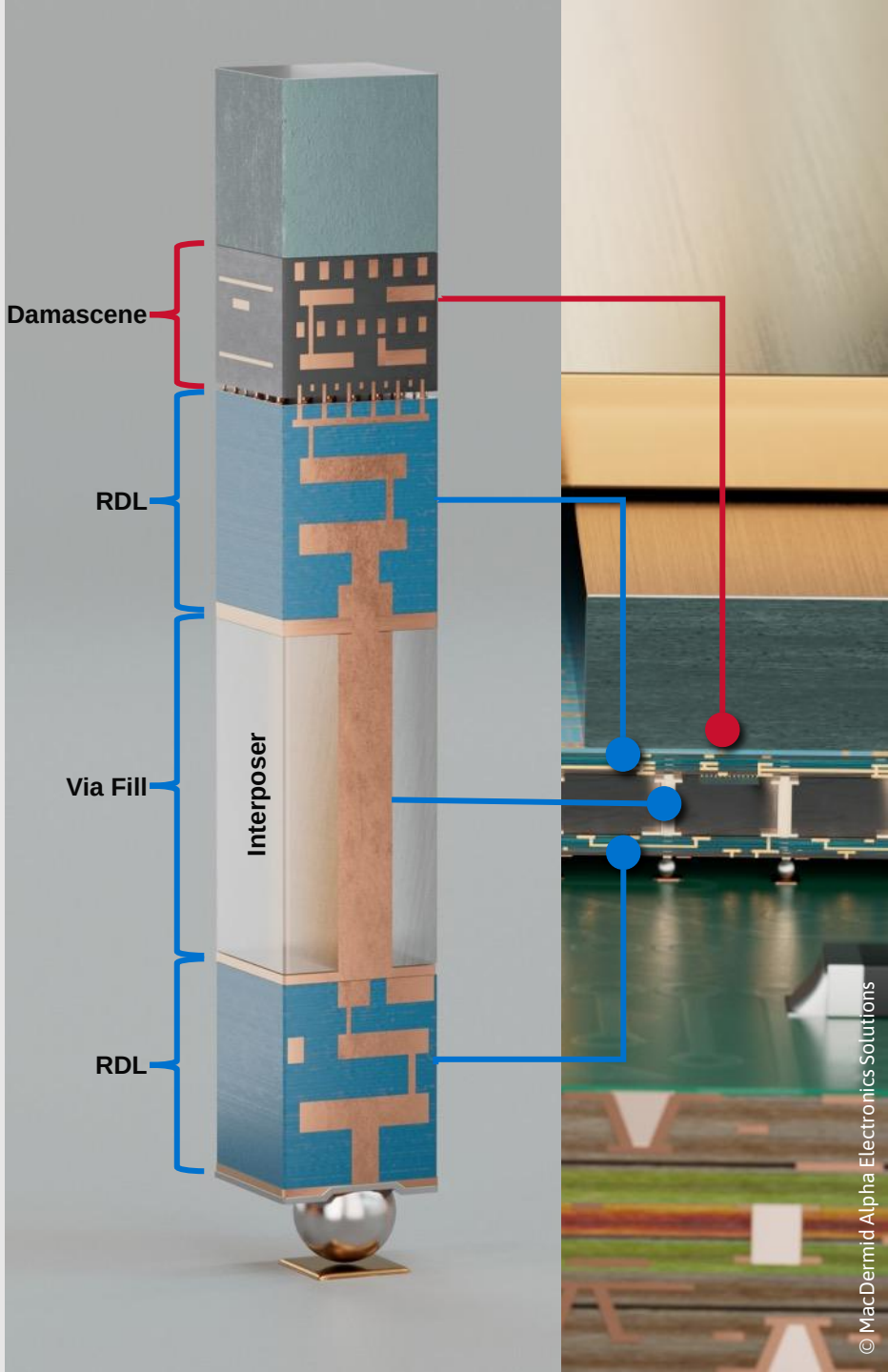
Damascene

- **Where is it used?** On-Chip-Level, IC Production
- **Challenge and Development:**
  - **Source Yole Group,** logic nodes below 5 nm are projected to account for over 20% of global wafer volume by 2027, with 2 nm entering full-scale production in 2025–2026
  - PVD-Processes struggle to achieve a uniform coverage of seed layers
  - New Chemistry Development are using a new alkaline system which enables electrochemical plating of such challenging structure without a seed layer

The Road to Finer Pitches

From 130nm to 2nm

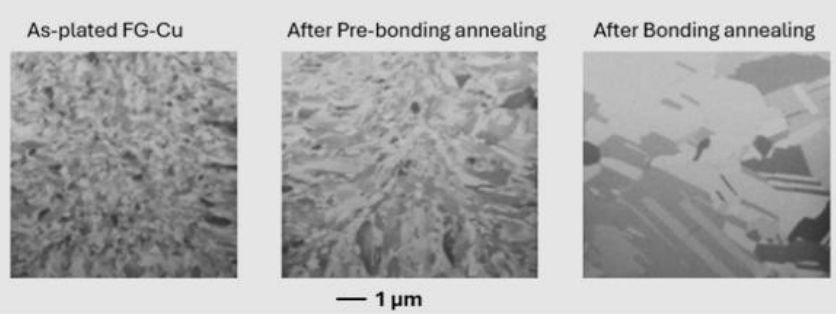




Interconnect Technologies

Hybrid Bonding

- **Principal,** Atomic diffusion between Cu-to-Cu Oxide
- **Benefits:**
  - **Pitch <10µm,** enabling up to 1Million connections per mm^2
  - **Low Resistance, High Reliability, High Energy Efficiency**
  - **No Induction-Effect,** HF and High-Switching-Speed
- **Used in:**
  - 3D Stacking for Die-to-Die or Wafer-to-Wafer
  - Chiplet Integration on High Density Die-to-Die
- **Challenges:**
  - Package alignment in Nano-Meter-Range
  - Grain structure of copper → Target fine grains, <0,2µm for processing



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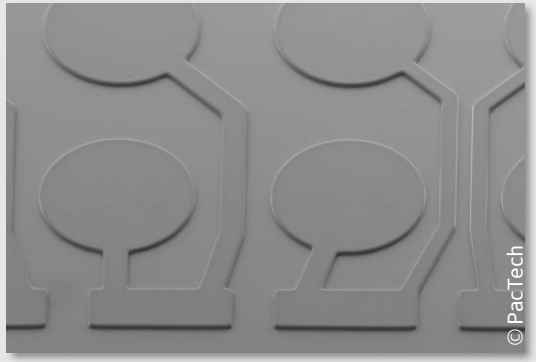
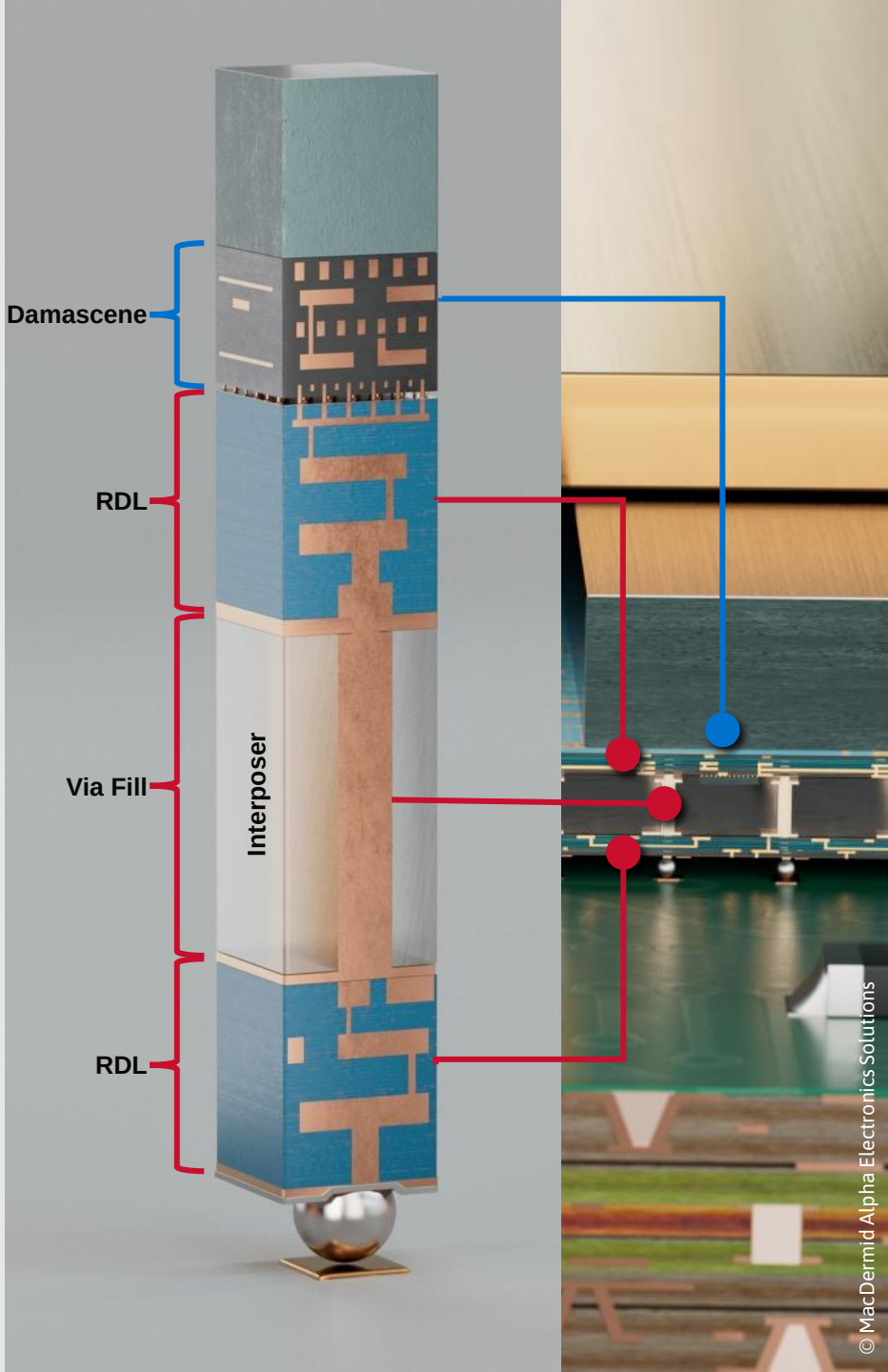
Interconnect Technologies

Random-Distribution-Layer (RDL) and Via-Filling Materials

- **Random-Distribution-Layer:**
  - **Where is it used?** Packaging-Level, Post-Wafer
  - **Redirection** and **Rearrangement** of I/O contacts to connect Chip to package and substrate in µm-range

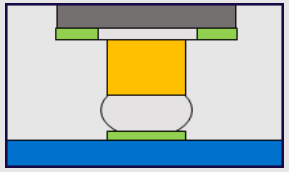


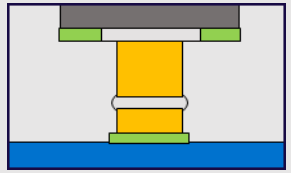
- **Through-Silicon-Via:**
  - **Where is it used?** Packaging Level, Mid-End
  - Used for **vertical Die-to-Die** Connections
  - **Challenges, CTE-Mismatch** Cu to Interposer material, **Yield-improvement** by using robust galvanic chemicals and processes, **Costs**

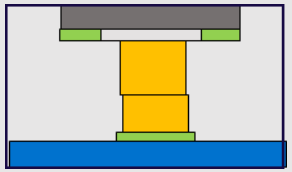


Interconnect Technologies

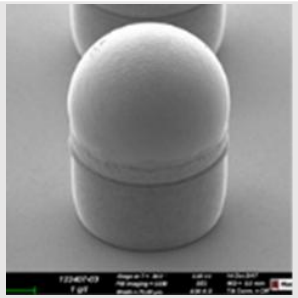
Bump, Micro-Bumps, Pillars

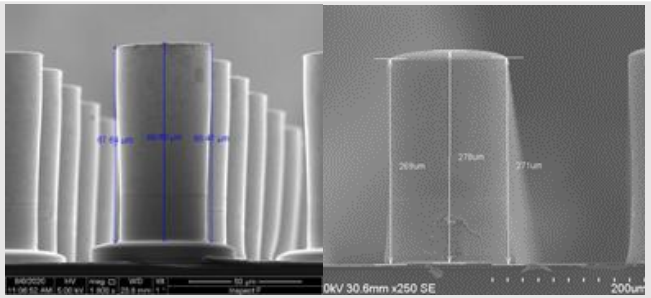






Bonding Method	C2 FC with Cu Pillar	Thermal compression FC with Cu Pillar	Thermal compression FC
Bump Pitch	140 ~ 60 µm	80 ~ 20 µm	<30 µm
Bump Metallurgy	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu





Finer pitch, Current carrying, Thermal performance, Reliability, Signal integrity

Interconnect Technologies

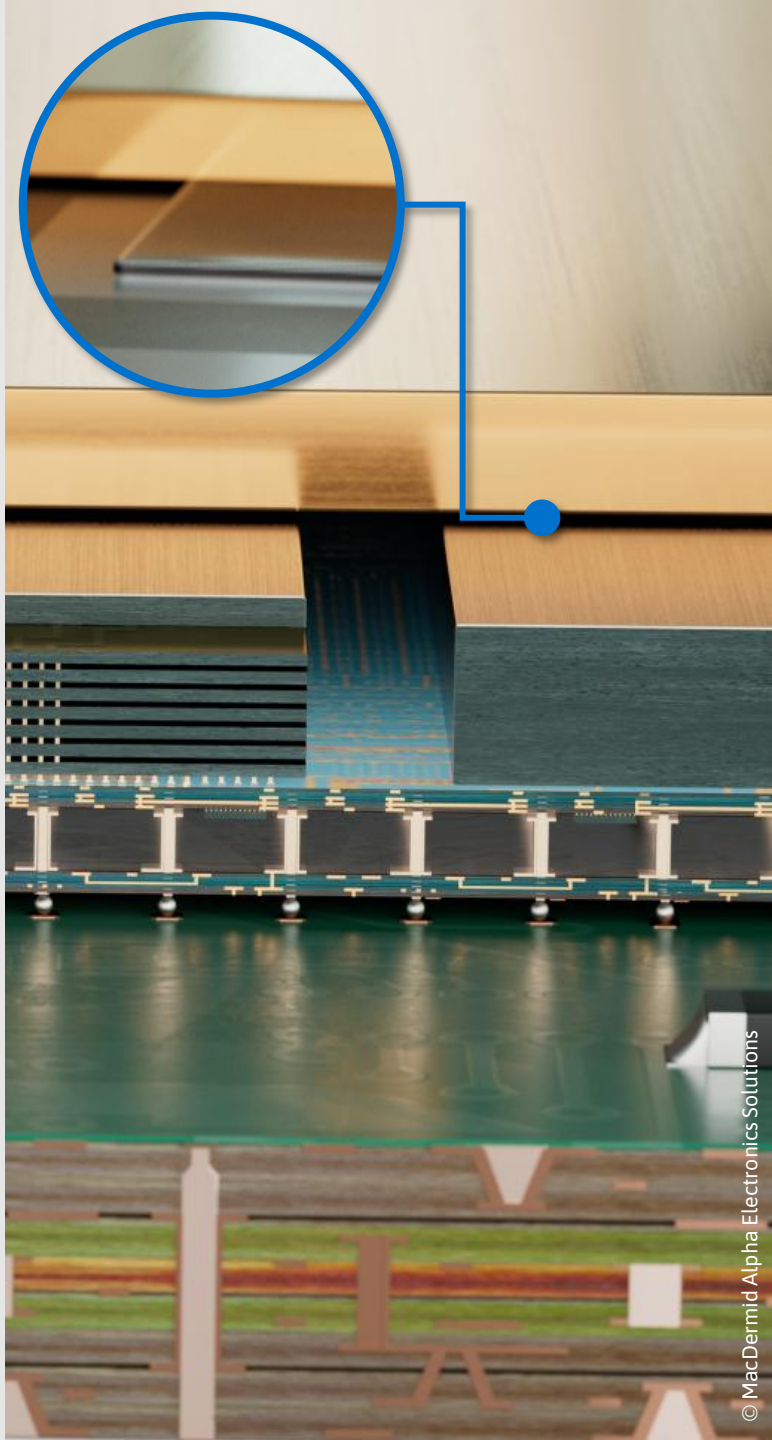
Low-Alpha Tin

- **Challenge and Development:**
  - High-density Packages can be sensitive to radiation exposure.
  - Effects are Soft-Errors in Flip-Chip, SiP or Memory-Packages
  - Low-Alpha Tin (Sn) can mitigate or eliminate this influence.
  - Main source radioactive isotope Pb-210 with half-life-period of ~22years.
  - Development of specific refining processes, controlled supply chain, material selection with aged tin, verification methods to test α-emmisions of the final product.
  - Tin-variants
    - Standard Sn: 10-100 $\alpha/cm^2 \cdot h$
    - Low-Alpha Sn: 0.002-0.02 $\alpha/cm^2 \cdot h$
    - Ultra-Low-Alpha Sn: <0.001 $\alpha/cm^2 \cdot h$
- **Benefits:**
  - **Improvement** of **Signal-Integrity**
  - **Increased Reliability** in HPC, Automotive Safety and Memory-Systems
  - Fulfillment **JEDEC-requirements** e.g. JESD97A, JESD89A

Thermal Solutions

Enabling High Performance Applications

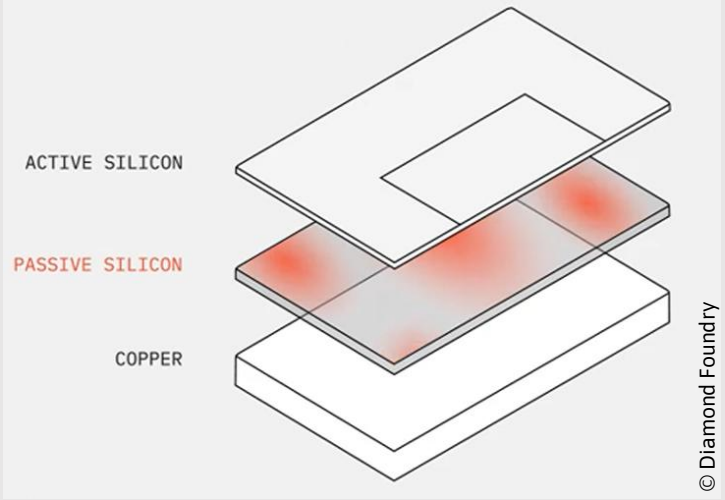
- **Power Density:**
  - **Increase** of functionality leads to higher heat output
  - **Modern** HPC- or Ai-**Packages** already reached **>1W/mm²**
  - **Uneven power output** reinforces **hotspot** effects
- **Reliability:**
  - Uneven **Hotspot distribution** creates temperature gradients within the packages
  - **Increase** of **Mechanical Stresses** and **Degradation** on the packages
- **Challenges and Trends:**
  - **Improvement** on **Rth-Path** for the complete package
  - **Reduction** of **Interfaces** or **Improvement** of their quality
  - Usage of **New Materials, Spreader** and **Cooling** solutions



Thermal Solutions

Enabling High Performance Applications

- **Reinventing, Re-Designing,** and using **New Materials** in this type of application
- Introduction of **Diamond Substrates** and **Silver Sintering** Technology
  - **Increase** of **Thermal Conductivities (X-Y-Z)** of **Spreader** and **Interconnection Material**
  - **CTE-Adjustment**



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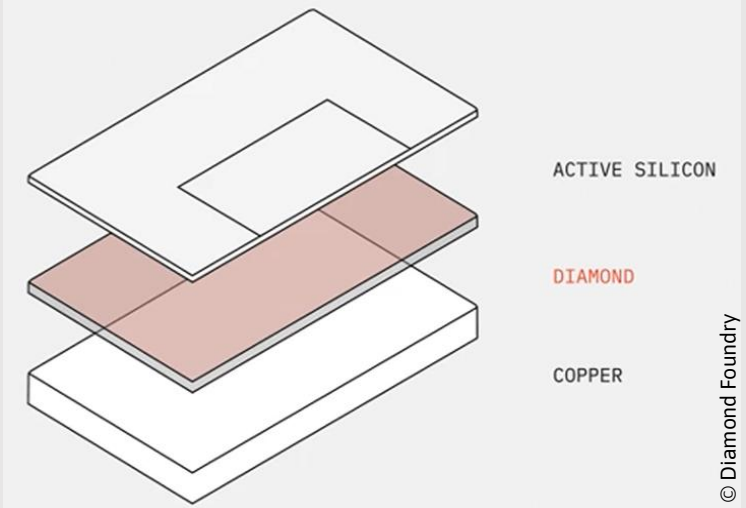

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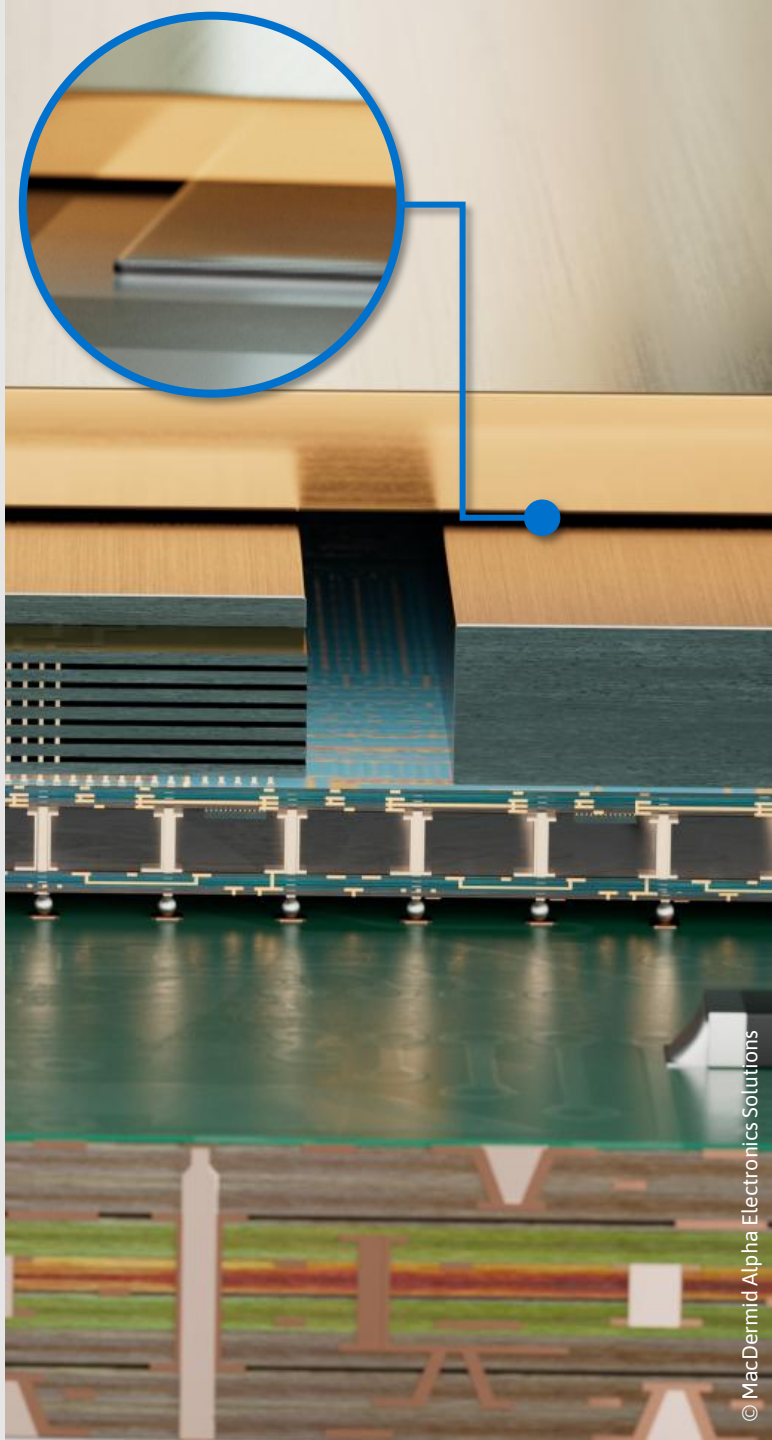
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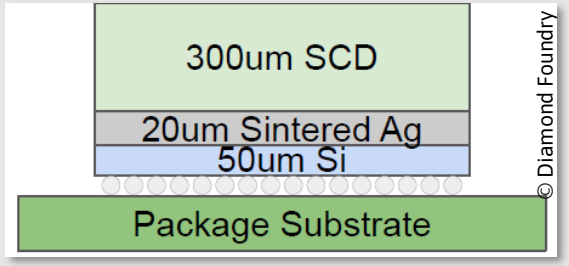
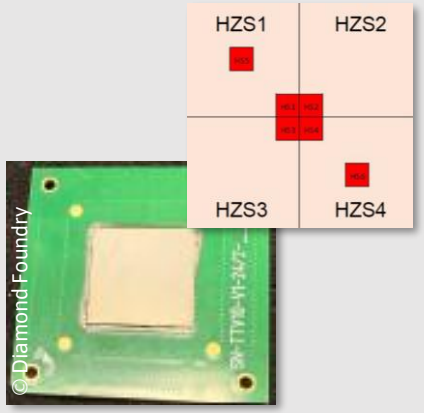
MacDermid Alpha ELECTRONICS SOLUTIONS DIAMOND FOUNDRY

Thermal Solutions

Enabling High Performance Applications

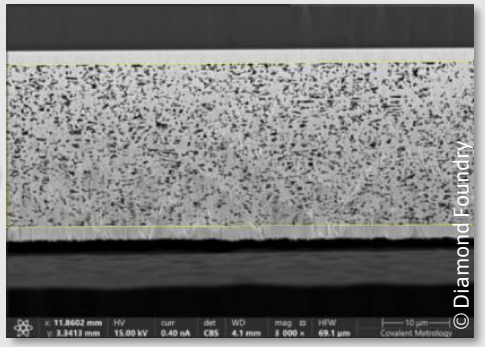
- **Test Vehicle and Setup**

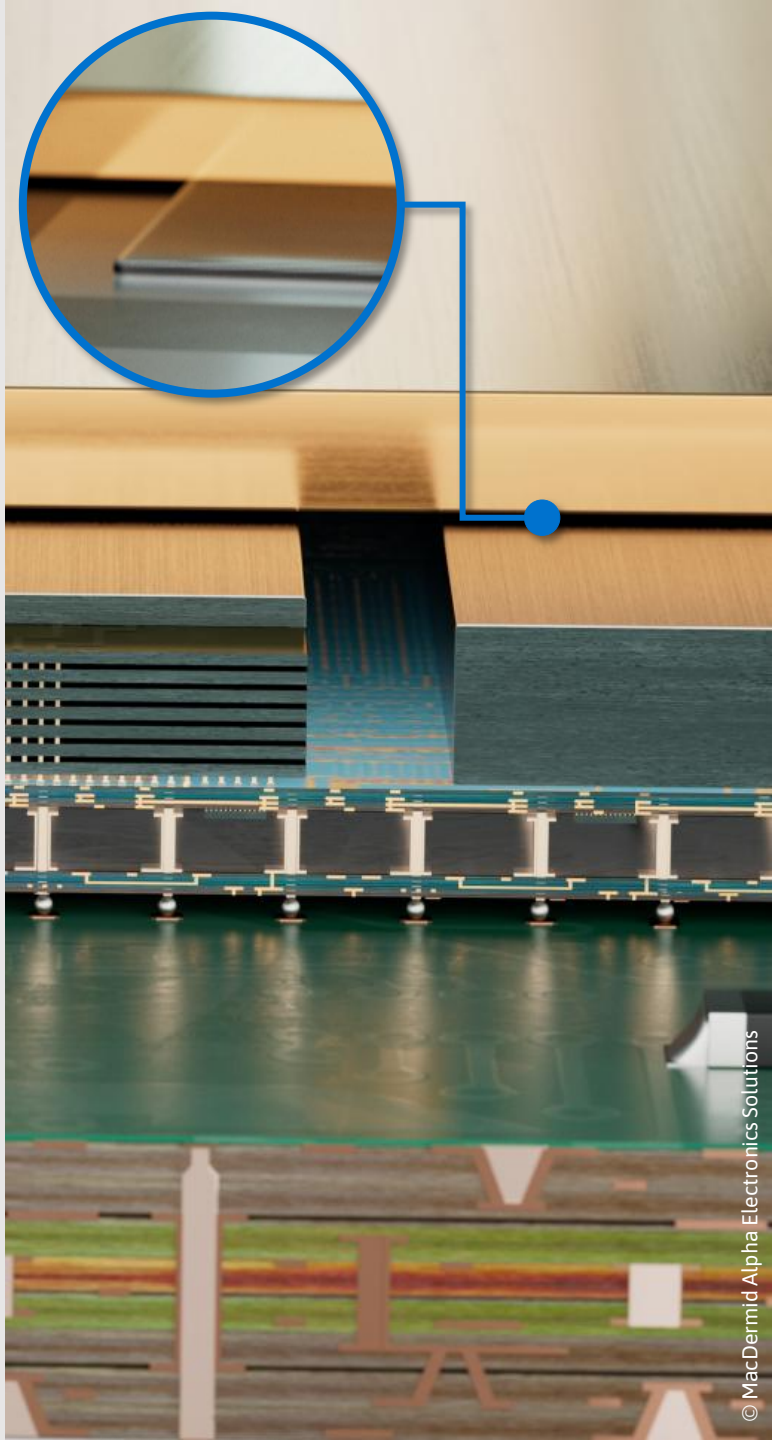




SCD grinding and wafer dicing → Ag sintering SCD2D → Assembling and eTest

- **Low Sintering Pressure** through the use of **Nano-Scale-Particles**
- **Uniform and Co-Planar layer** through the use of **Films and Preforms**





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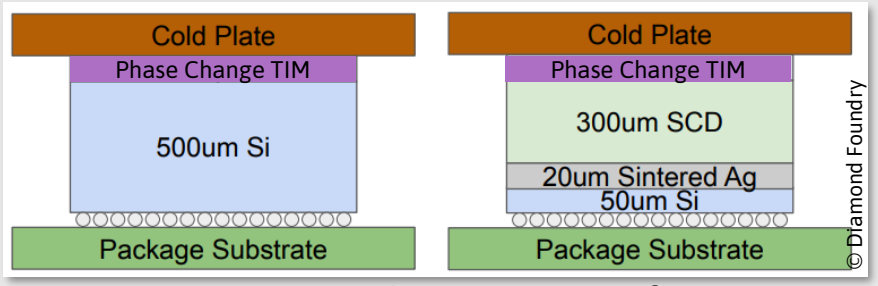
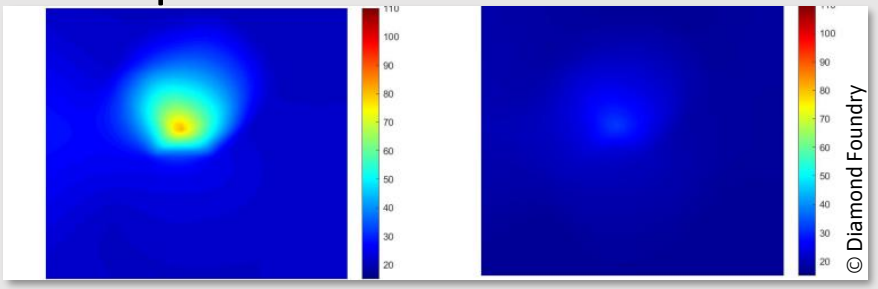
Thermal Solutions

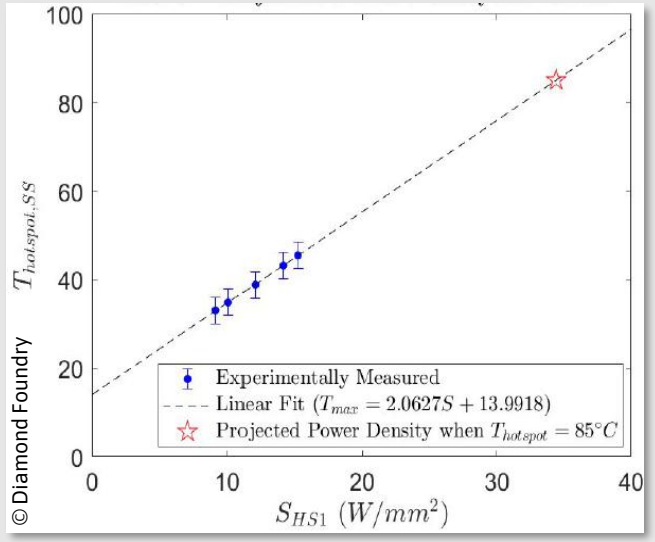
Enabling High Performance Applications

- **Test Results**

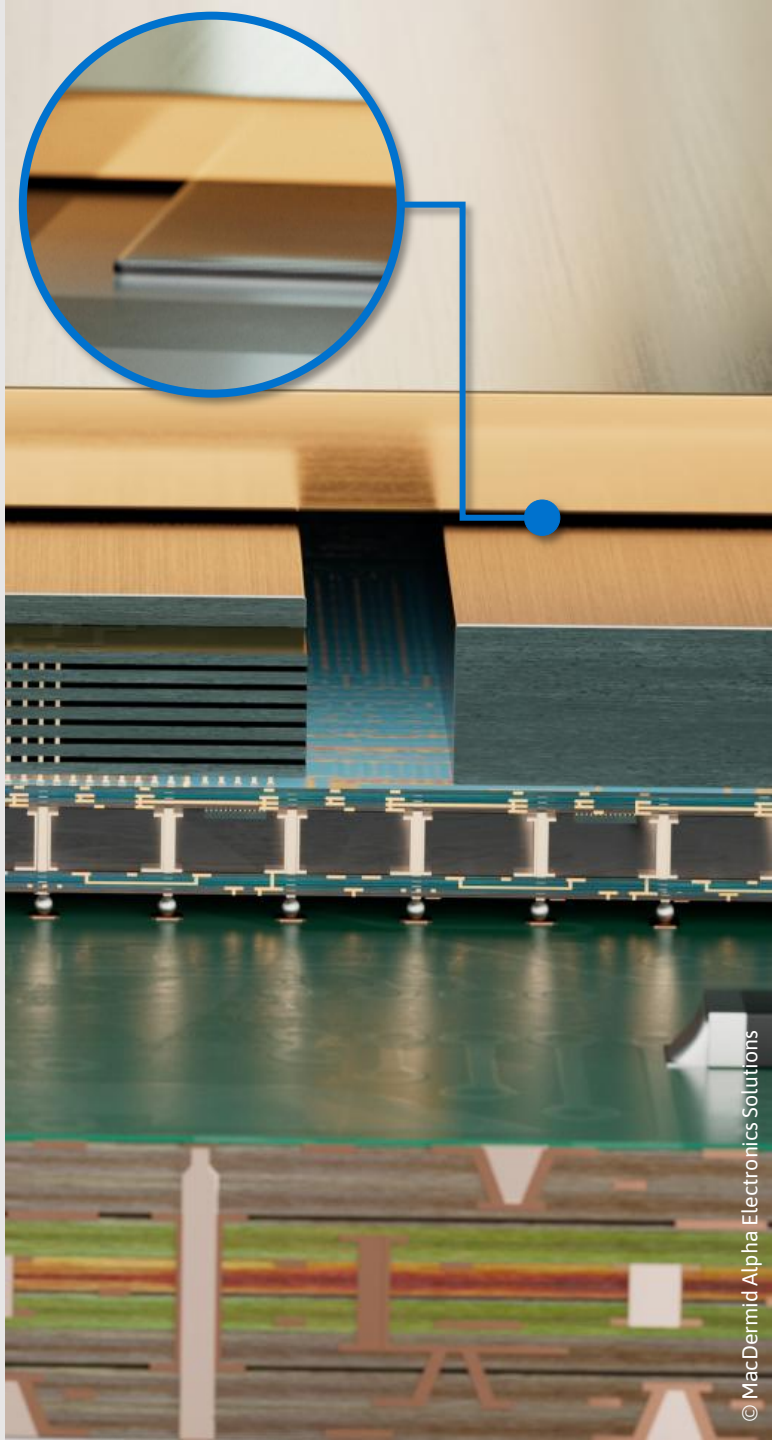


Experiment for 6.25mm² HS1





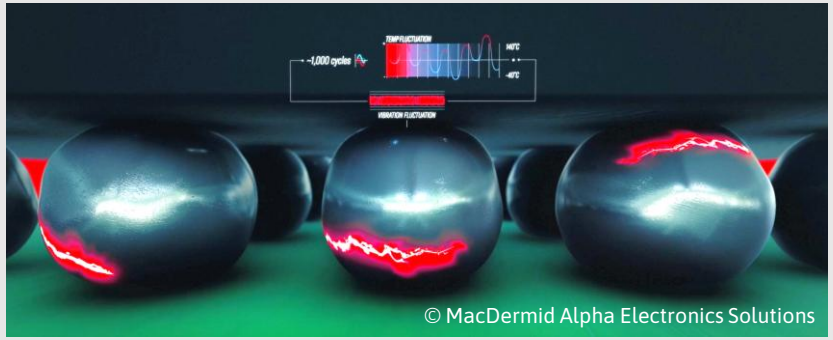
- **52K Reduction** at 9.2 W/mm²
- **Projected 3.8x Increase** in **Power Density** @ 85°C
- **Projected Power Density** at 85°C of **34.4 W/mm²**

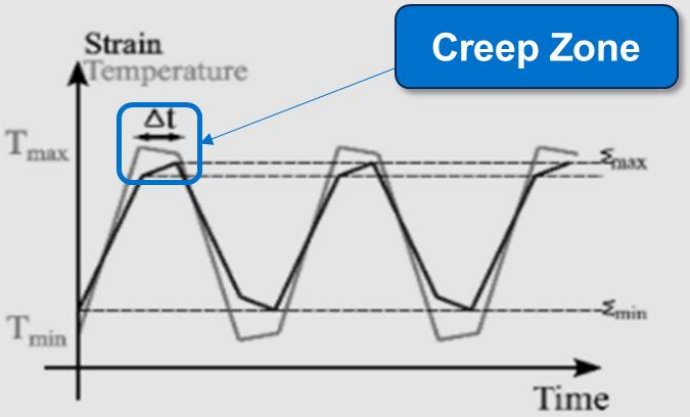


Interconnection Material

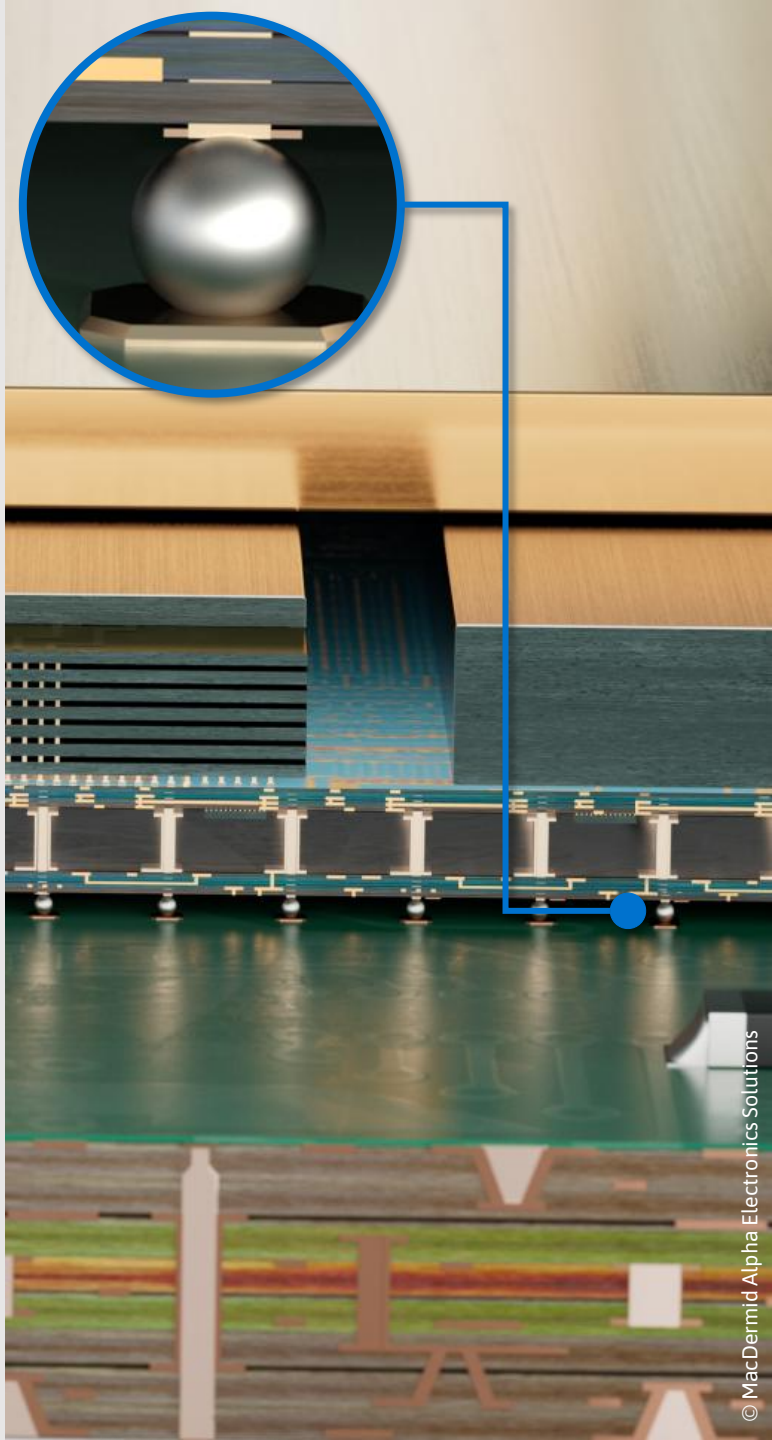
Package Interaction with PCB Assembly

- **Challenges and Trends:**
  - The trend toward smaller structures, thinner packages, and higher I/O density is extending to other package forms e.g. BGAs.
  - **Reduced stand-off heights** result in **increased** mechanical and thermal **stress**.





  - **New alloys** are being developed to **better tolerate** the increased **stresses**.
  - The focus is on modifying grain boundaries, diffusion behavior, and hardness characteristics.



Closing

- Moore's Law has driven semiconductor innovation for more than five decades.
  - **Original formulation (1965):** ***The number of transistors on an integrated circuit doubles approximately every 12 to 24 months, while the cost per function remains constant.***
- Scaling is reaching its physical and economic limits.
- Transistor technologies are largely mature – further miniaturization requires extreme investment.
- Innovation now happens at the system level.
  - Advanced Packaging, Chiplets, 2.5D/3 Integration, and SiP.
  - Materials, interconnects, and thermal management are becoming decisive performance enablers.
- Industry must remain technology-open
  - to explore non-traditional approaches and unconventional material combinations.
  - fostering progress beyond classical scaling boundaries.
- Future progress = smarter, cross-disciplinary integration – not just smaller transistors.

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Thank you for your attention!