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Conference & Exhibition

Keynote speaker: Stefan Chitoraga

Job Position: Technology & Market Analyst specializing in semiconductor Packaging and Assembly

Company: Yole Group

Title of the presentation:

Advanced Packaging Market Outlook, technology trends and how Europe positions itself for this business.

Short CV:

Stefan Chitoraga is Technology & Market Analyst specializing in Semiconductor Packaging. Within the Manufacturing & Global Supply Chain activities at Yole Group, Stefan is focused on advanced packaging platforms and processes, substrates, and PCBs. He is involved daily in the production of technology & market products and custom consulting projects.

Prior to Yole Group, Stefan served as a package design engineer at Teledyne E2V for 4 years, where he oversaw the ceramic package and glass lid development for

image sensors, developing mechanical design, routing, electrical and thermal simulations. Furthermore, he spent 2 years at STMicroelectronics where he developed a new IC Substrate design, for organic package for SerDes applications.

Stefan holds a Bachelor’s in electronics and computer science for industry applications from the Polytech Grenoble (France).

Abstract:

Advanced Packaging has become critical and effective increasing device performance and bandwidth, reducing the gap between Si and PCB. This keynote delves into the Advanced Packaging Market Outlook and technology trends. On top of that an analysis related to Europe’s position in this business will be discussed.

There is a strong growth in high-performance computing, cloud computing, networking, artificial intelligence, autonomous driving, and personal computing applications. Simultaneously, there are die power improvements at escalating cost associated with more advanced nodes, resulting in bigger and more complex dies. These trends triggered semiconductor industry to strategize system-level scaling with high-end packaging solutions instead of purely scaling FE advanced nodes. Heterogeneous integration is a potential path forward to optimize the scaling cost by partitioning SoC chips and scale only those most critical circuit blocks. Therefore, advanced packaging technologies with high interconnection density, high bandwidth, and high-power efficiency are needed. Chiplet & Heterogeneous integration is a potential path forward to optimize the scaling cost by partitioning SoC chips and scale only those most critical circuit blocks. Therefore, advanced packaging technologies with high interconnection density, high bandwidth, and high-power efficiency are needed.

This presentation will be particularly beneficial for specialists in electronic packaging who are looking to enhance their understanding of the market and technology trends as well as market outlook for advanced packaging.