Keynote speaker: Syhem Larguech
Job Position: Application Engineer

Company: Cadence Design Systems

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Title of the presentation: Advanced IC packaging in the context of multi-chiplet based architectures.

Short CV:

Syhem Larguech received the Dipl.-Ing. degree in electrical engineering from the National Engineering School of SFAX (ENIS), Sfax, Tunisia, in 2012. She earned a PhD degree in Microelectronic Systems from the University of Montpellier, Montpellier, France, in 2015. In 2016, she joined the Interuniversity Microelectronics Centre (IMEC), where she was involved in IC package design and electrical analysis for various applications such as space and high speed. Since September 2019, she has been with Cadence Design Systems in Munich, Germany, where she currently works as an application engineer, supporting Cadence users in the development of their IC packaging projects. She is also actively engaged in the design of advanced IC packages for Cadence's internal hardware products, such as the Palladium platform. Her primary interests revolve around advanced IC packaging technologies, modelling of IC packaging structures, and multi-fabric co-design automation.

Abstract:

The semiconductor industry is moving from monolithic chips to the world of 3D-IC, chiplets and stacked silicon and wafers. Advanced systems-on-chip (SoCs) are reaching reticle size limits, and as many companies now realize, simply following Moore's Law alone (More Moore) is no longer the best technical and economical path forward for the next wave of designs. As we approach the device scaling limitations at advanced nodes, the demand on compute performance and data transfer is at an all-time high. There has been a need to find innovative solutions to continue Moore's law scaling and achieve performance improvements with reduced power.

The semiconductor packaging industry is now poised to take on a larger, more significant role in electronic product design of the future. Stacking chips in the same package (3D) and a multi-chiplet system with silicon interposer on the same package (2.5D) are emerging as solutions of choice, which come with their own challenges.

To meet the market demand of the heterogenous chiplet-based architectures, new system level design methodologies are required, targeting system-level Power, Performance and Area (PPA). The Cadence Integrity 3D-IC platform is the industry's first integrated solution for system planning, implementation, and accurate early analysis. It leverages Cadence's industry-leading implementation and signoff technologies for digital, analog, and packaging through a unified hierarchical database.