High Speed Signaling Challenges and Solutions for Electronic Packaging

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Outline

- High Speed Signaling (HSS) Trends for Electronic Systems
- Advances in Package Technologies – A HSS Perspective
- HSS Challenges and Solutions for Advanced Packaging
- Standardization for Package HSS
- Summary

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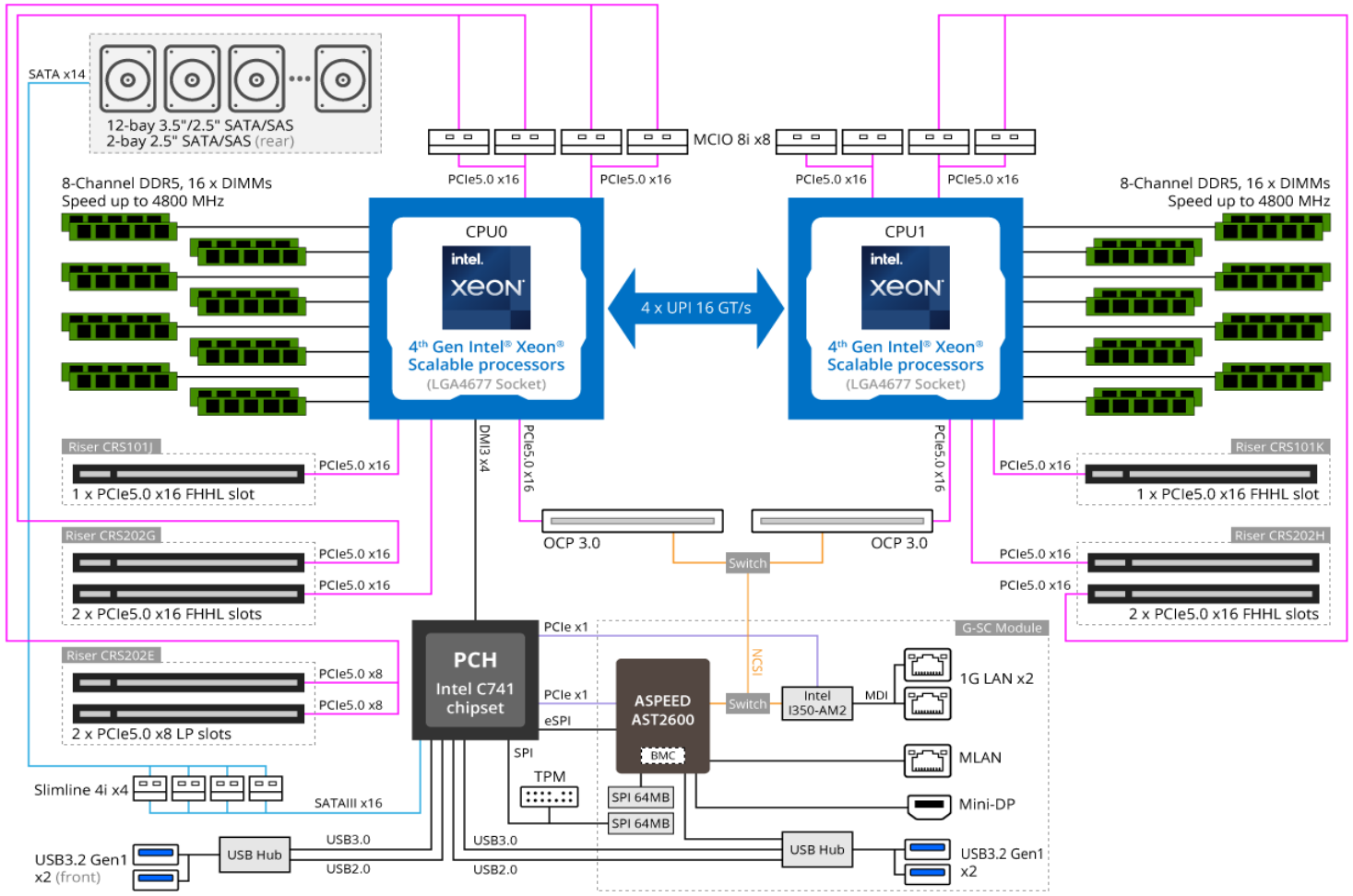
Input/Output (I/O) Interfaces for HSS

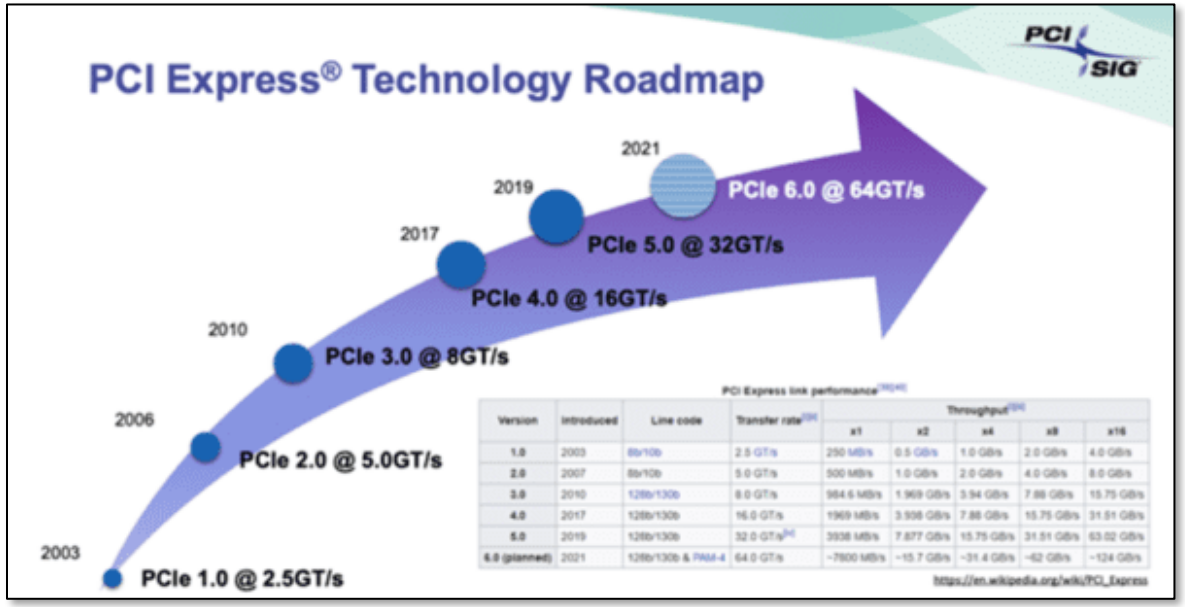
Example Data Center Server System Connectivity Diagram



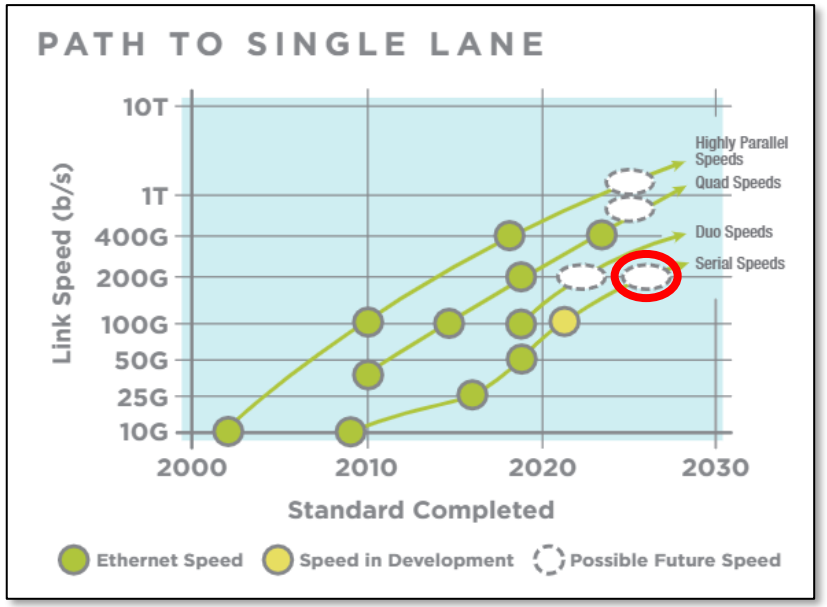
Source: Gigabyte

- Communication between components in an electronic system are provided by I/O Interfaces
- Various standards (DDR, PCIe, etc.) exist for off- *(and now also on-)*package I/O interfaces

Off-Package HSS Trends

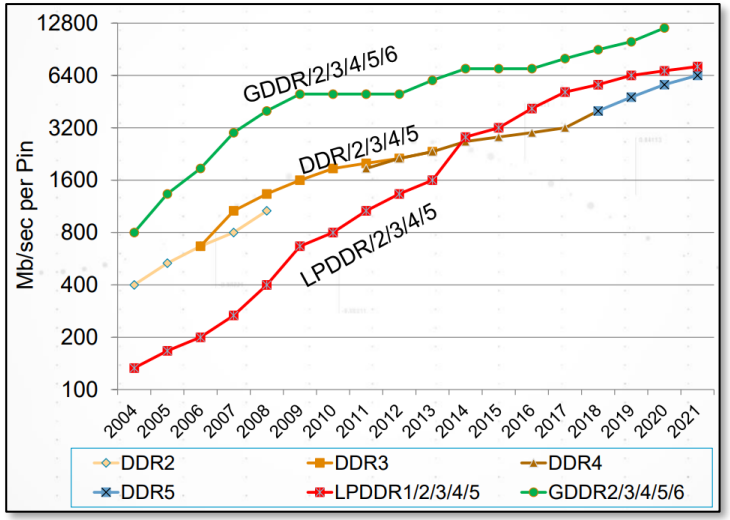


Source: PCI SIG



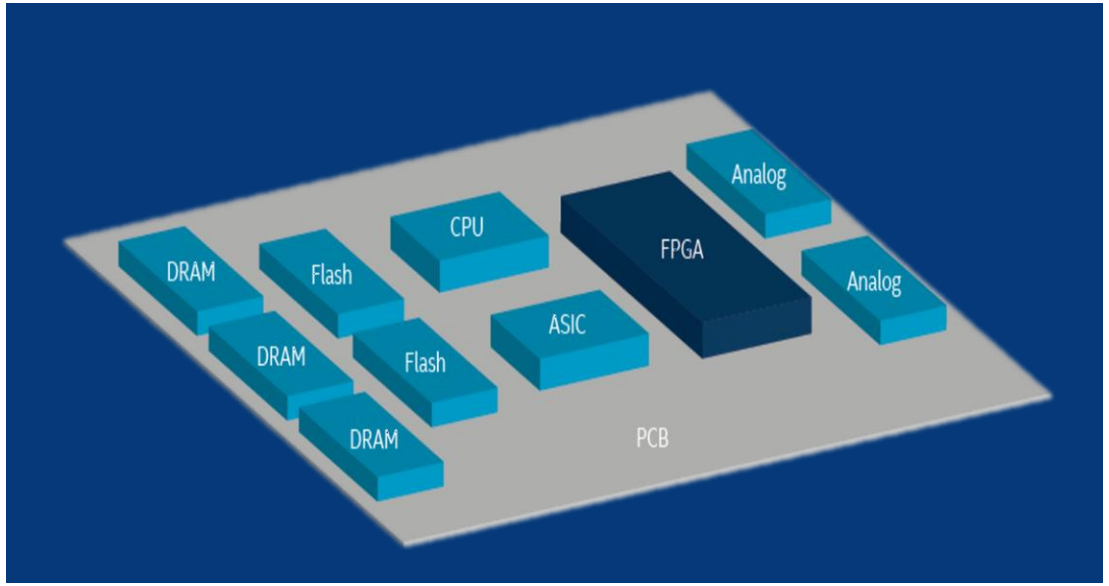
Source: Ethernet Alliance

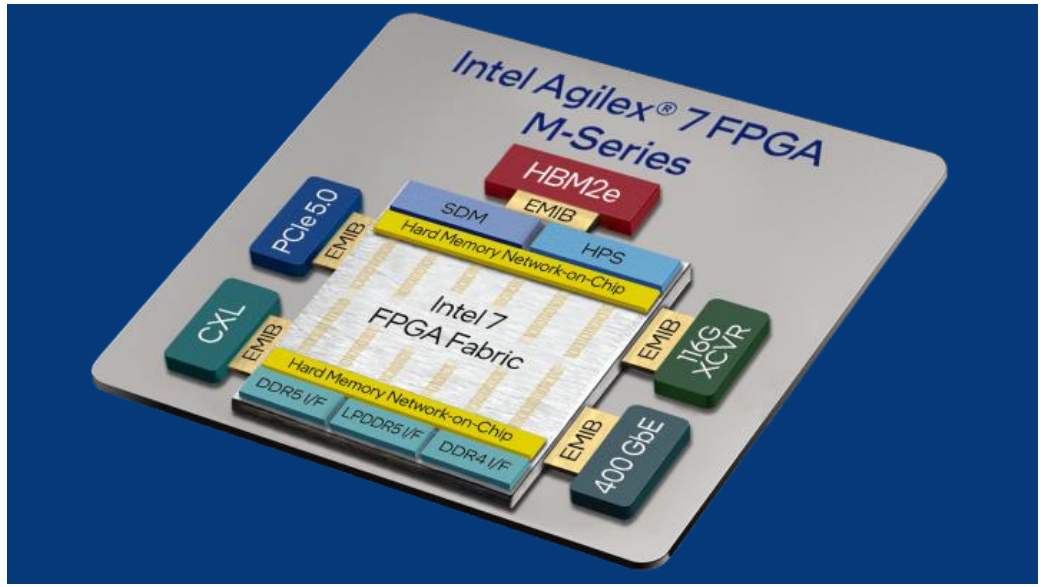
- Speeds for all off-package IO and memory interfaces are continuing to increase aggressively on a regular cadence
- Requires development of new interconnect technologies along with modeling, characterization, and design methodologies for these applications



Source: Keysight

On-Package HSS for Heterogenous Integration (HI)





PCB Integration

- Limited Interconnect Density → Limited BW
- Long Interconnects → Increased Power
- Large Form Factor

On-Package Integration

- Higher Bandwidth
- Lower Power & Latency
- Heterogeneous Integration of Multiple Nodes, Multiple IP, & Multiple Functions

- HI requires high bandwidth and low power & latency on-package connectivity
- Driving new interconnect technologies along with modeling, characterization, and design methodologies for these applications

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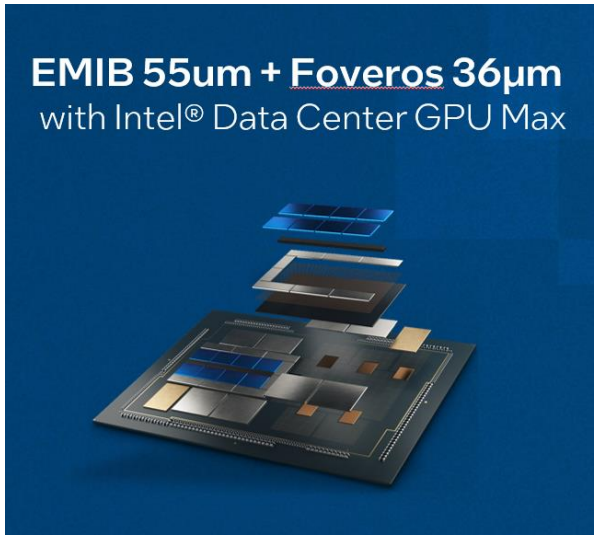
Recent Trends in Electronic Packaging

Traditional electronic package (CPU example)

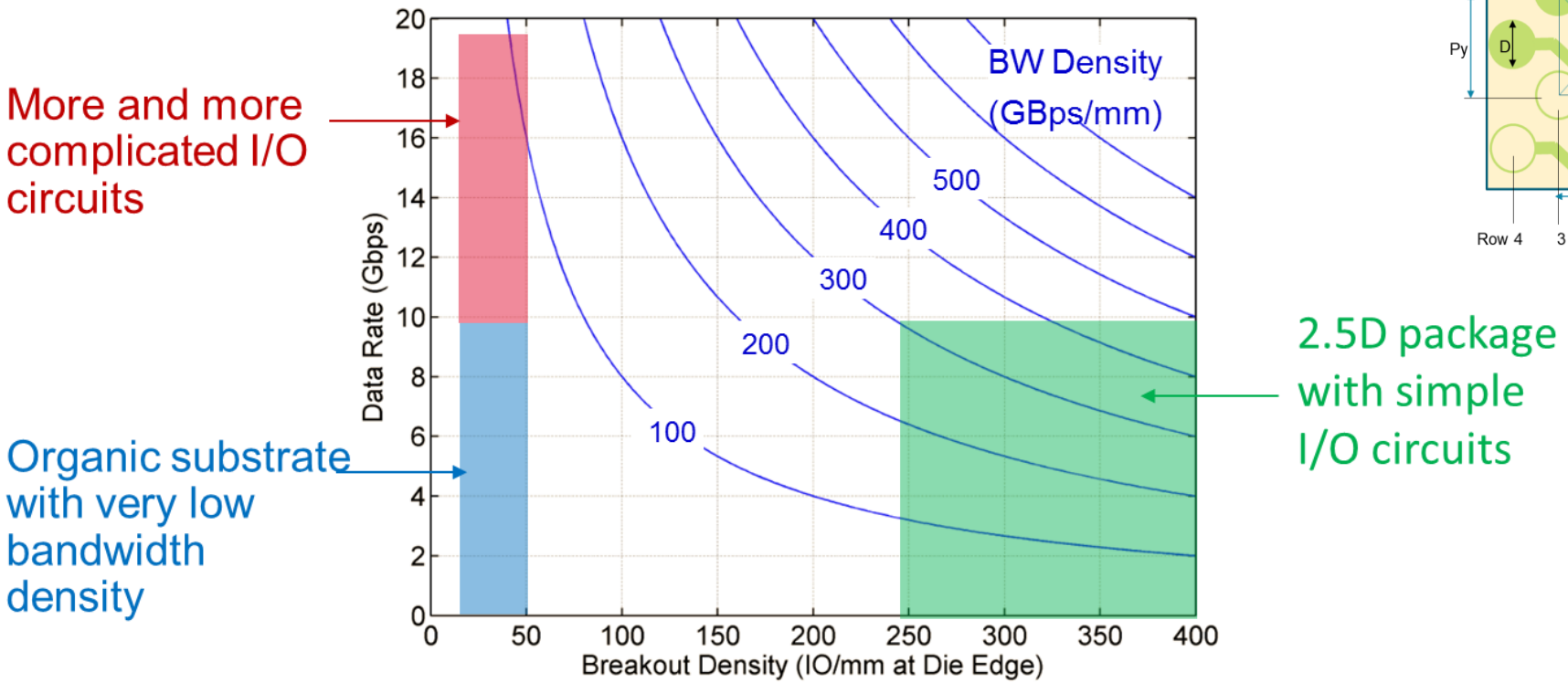


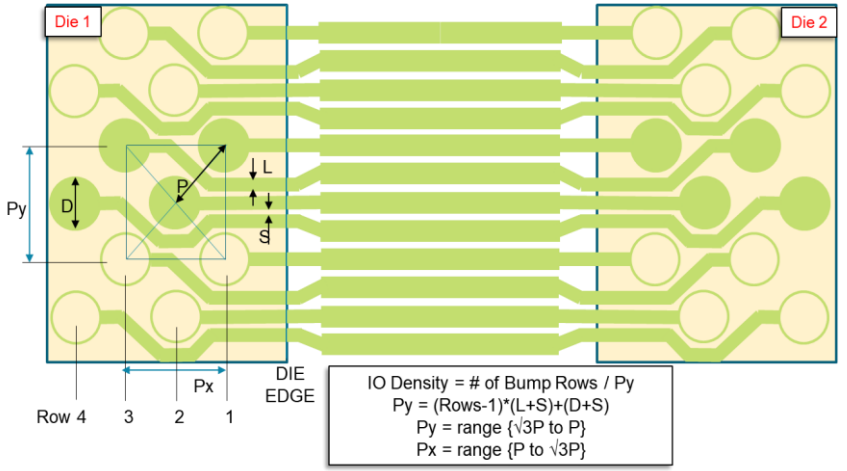
Advanced electronic packages (CPU/GPU examples)

- *Traditional electronic package*:
  - → Few dies
  - → Few layers
  - → Small form factor
  - → Simple architecture

- *Advanced electronic packages*:
  - → Many dies (or *chiplets*)
  - → Large number of layers
  - → Large form factors
  - → Advanced architecture:
    - → Much finer line width/spacing
    - → Higher IO/mm and IO/mm^2
    - → 3D stacking

Motivation for Advanced Architecture

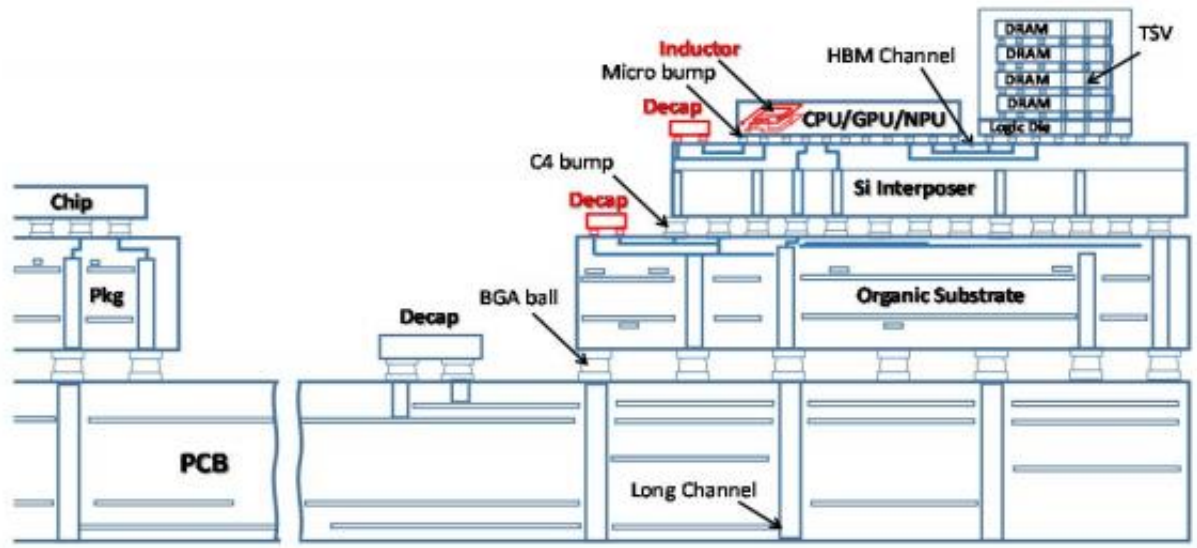


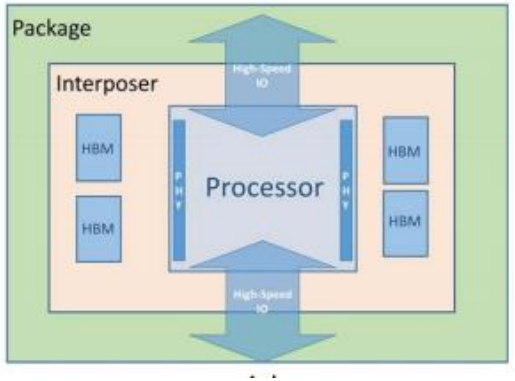


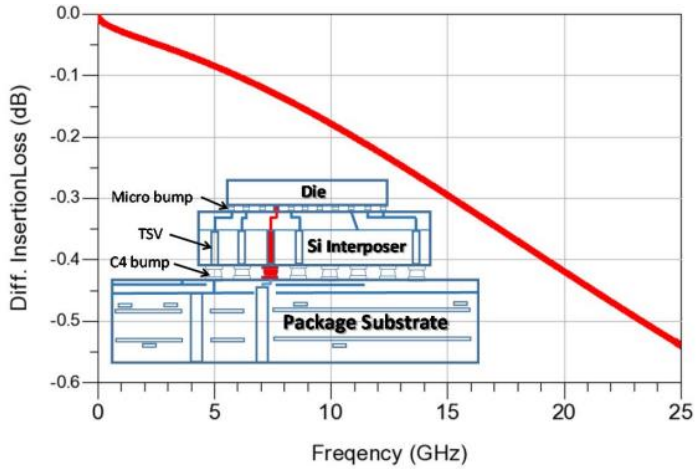
R. Mahajan et al., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 557-565

- To enable high bandwidth density connection between dies on a package with simple I/O circuits and low power consumption → Works for 'short' lengths!
- An 'advanced package' also has to accommodate off-package HSS scaling requirements with features such as low loss materials, HSS-optimized design rules, etc.

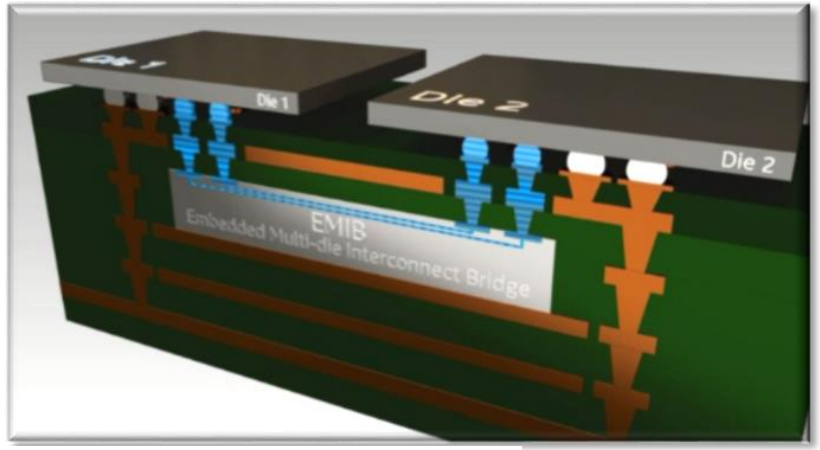
Advanced Packaging Examples (Silicon Interposer & EMIB)

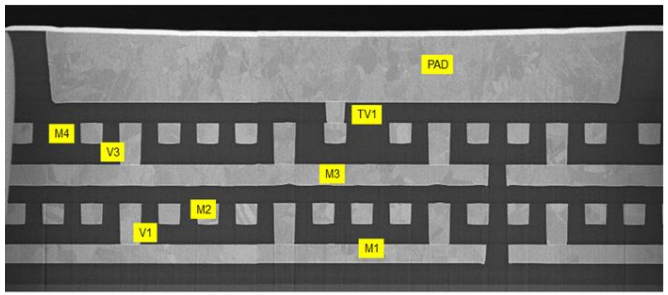


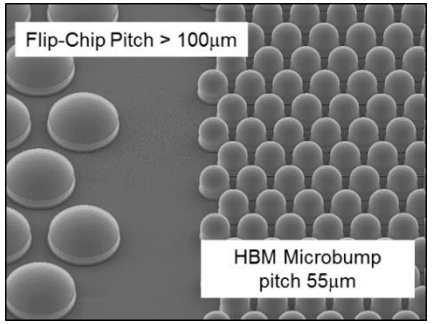


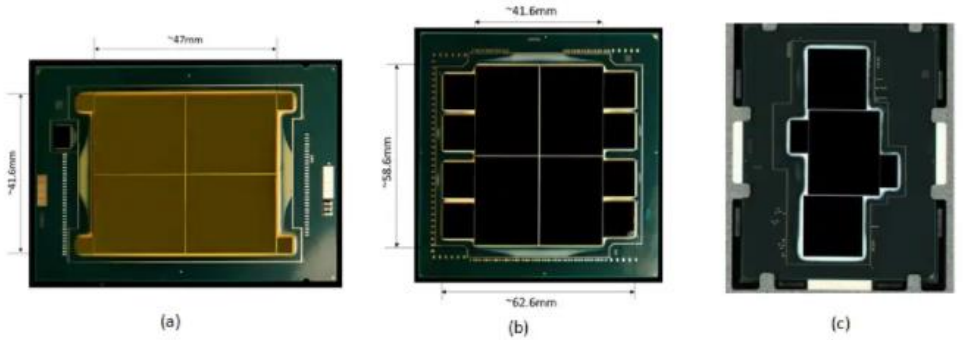


W. Beyene, N. Juneja, Y. Hahm, R. Kollipara and J. Kim, "Signal and Power Integrity Analysis of High-Speed Links with Silicon Interposer," 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), Orlando, FL, 2017, pp. 1708-1715
(Reproduced with permission of W. Beyene)









Various EMIB Package Configurations: In (a) and (b) the total Die Area is Substantially Greater than Reticle Size (c) shows an irregular and asymmetric Layout

Additional Reading

Heterogeneous Integration Roadmap

- **2021 Edition**
- 2020 Edition
- 2019 Edition
- ECTC 2019 Workshop Presentations
- Technical Committees
- Definitions

Heterogeneous Integration Roadmap 2021 Edition

Interested in hearing the latest updates and news on the Heterogeneous Integration Roadmap? Please sign up

Chapter 1 Overview

Chapter 2 High Performance Computing

Chapter 3 IoT

Chapter 4 Medical, Health

Chapter 5 Automotive

Chapter 6 Aerospace & Defense

Chapter 7 Mobile

Chapter 8 Single Chip & Multi Chip

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https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

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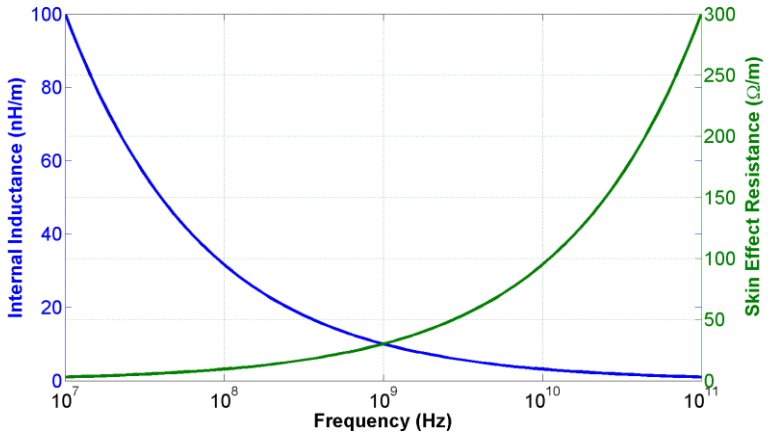
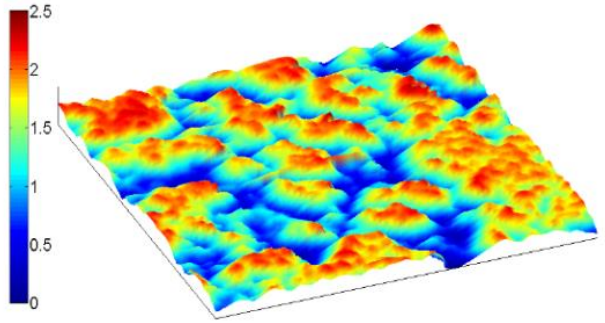
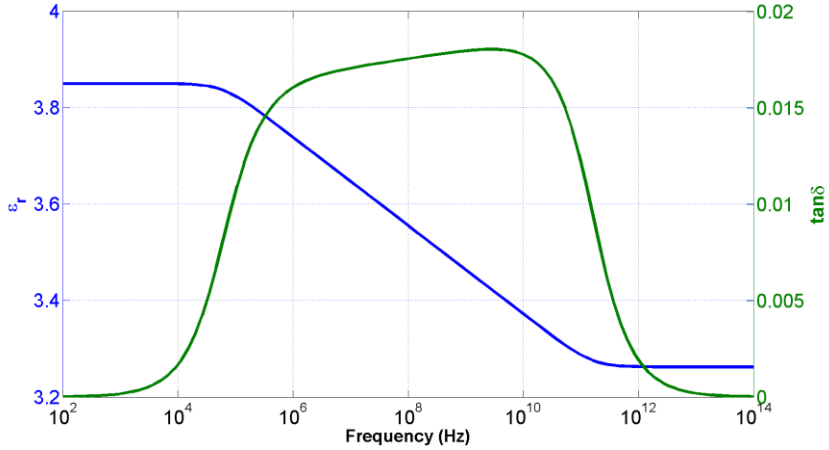
Package HSS Modeling and Characterization Challenges

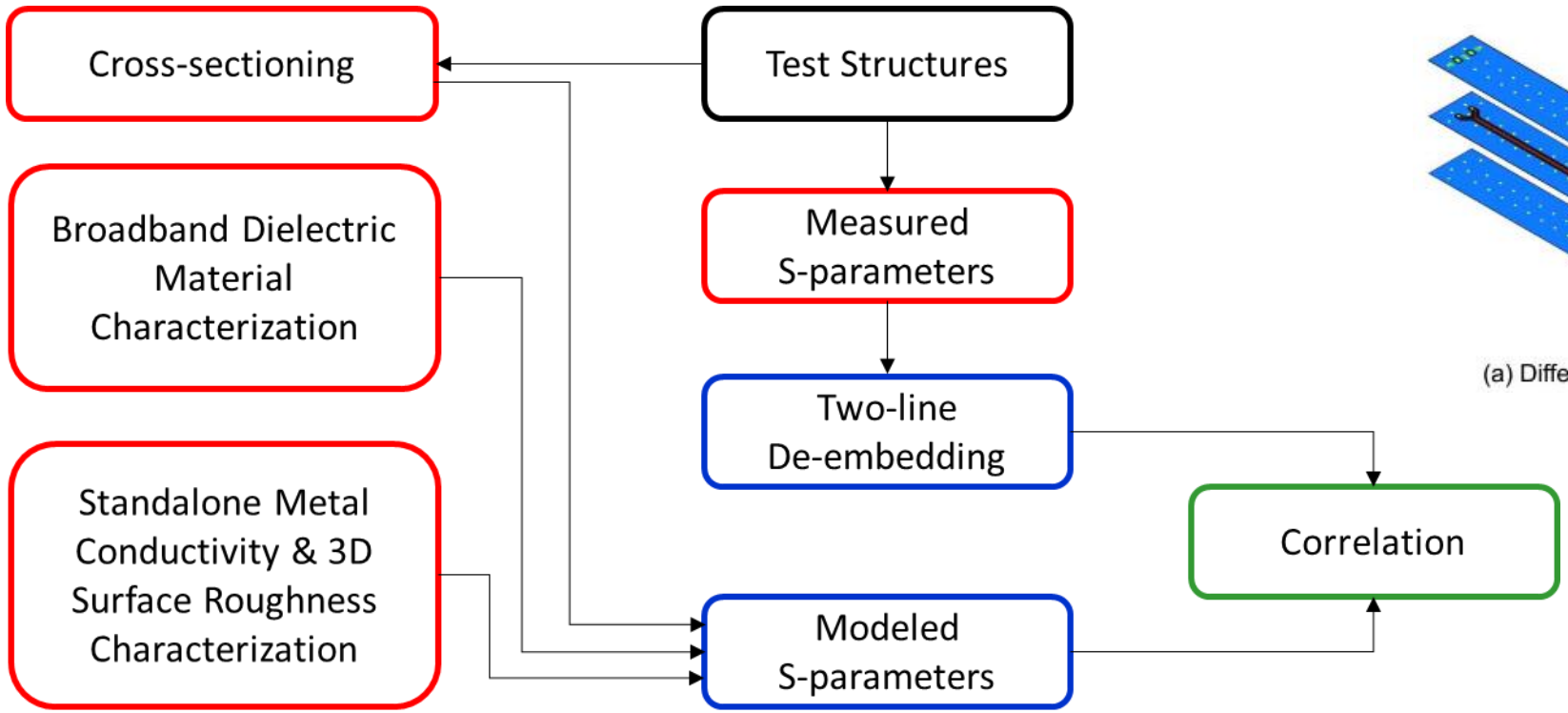
- As data rates increase and margins decrease, new phenomena that were insignificant in the past designs become significant
  - Frequency dependence of resistance losses and inductance for conductors
  - Non-ideal effects of the copper surface
  - Frequency dependence of dielectric permittivity and loss tangent
  - ***New geometrical scales with new materials and processes introduced by HI***
- We need *validated models* that accurately predict these effects

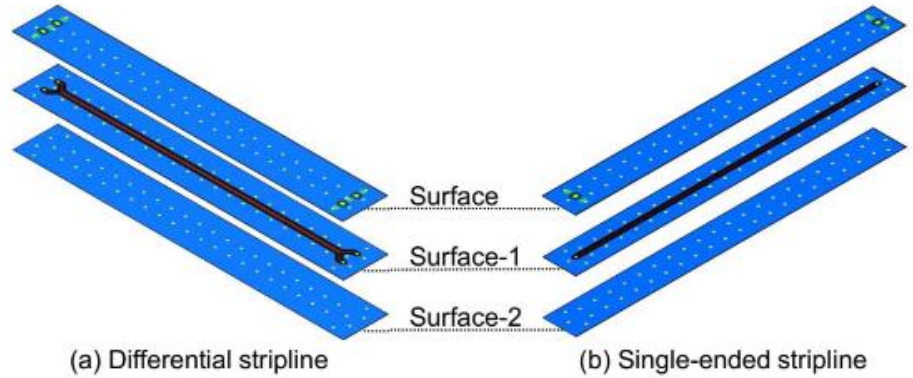






Package HSS Modeling-to-Measurement Correlation



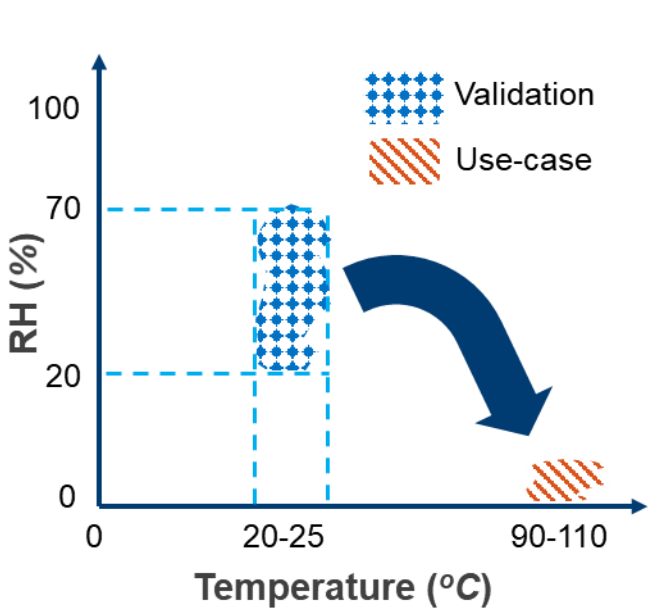


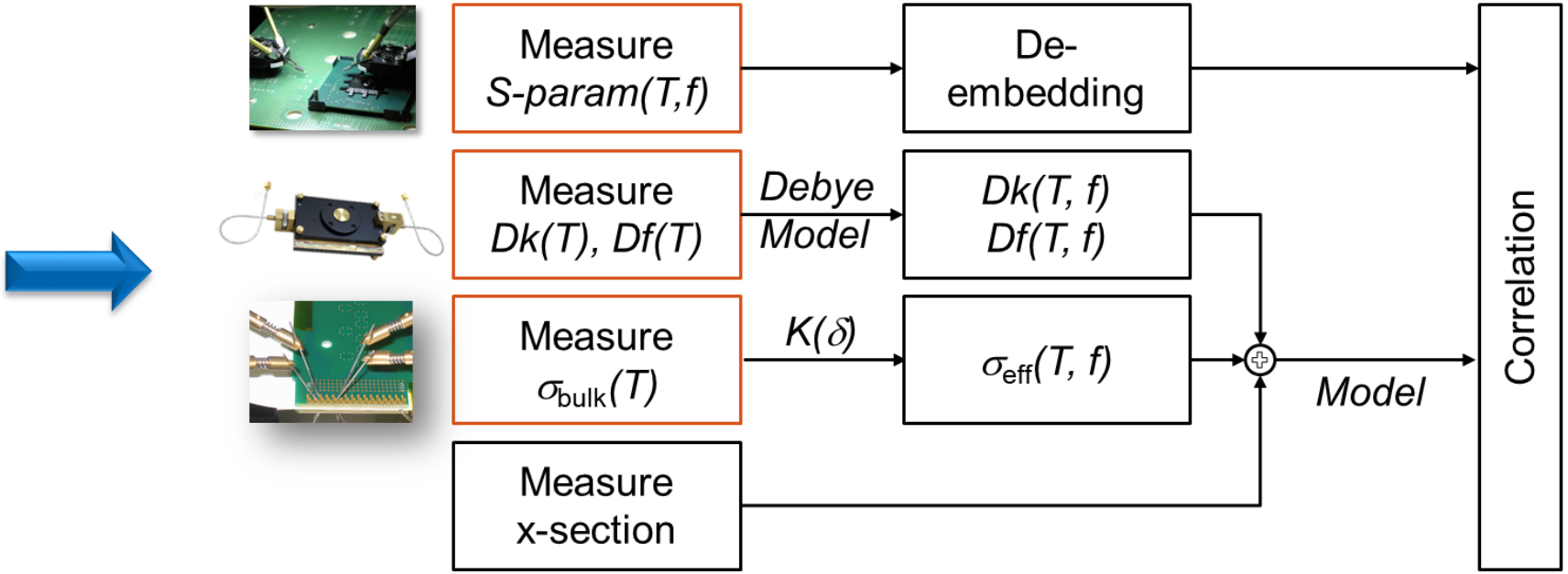
Example package interconnect problem

C. S. Geyik et al., "Improved Package Modeling and Correlation Methodology for High Speed IO Design," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 985-991

- Comprehensive flow for an improved package modeling and correlation methodology is essential for efficient electrical design

Impact of Environmental Conditions

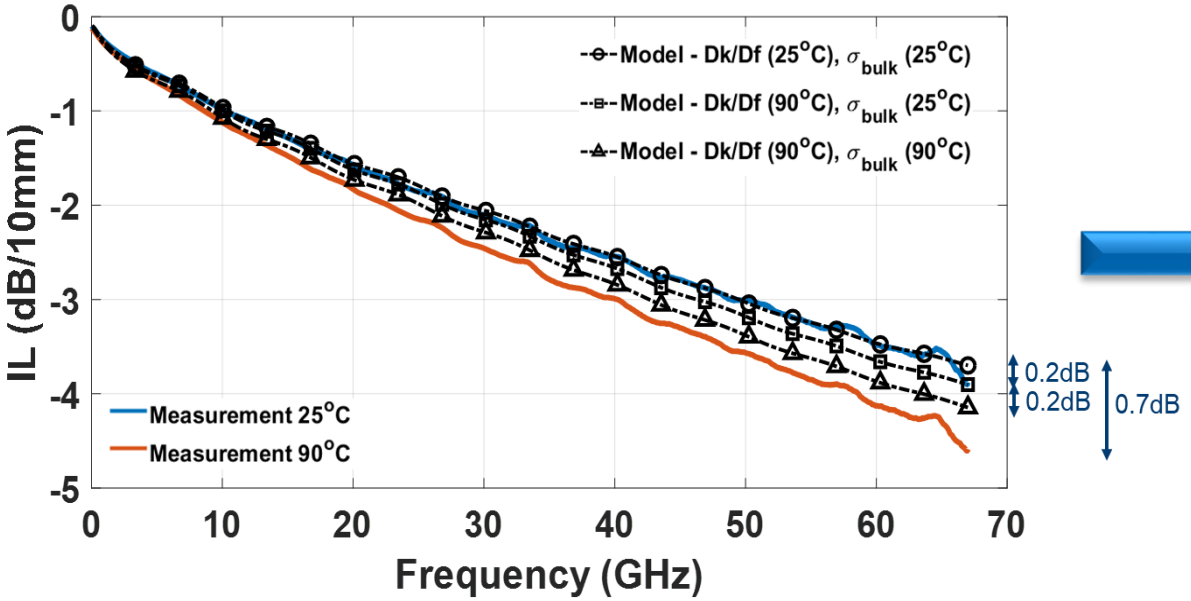


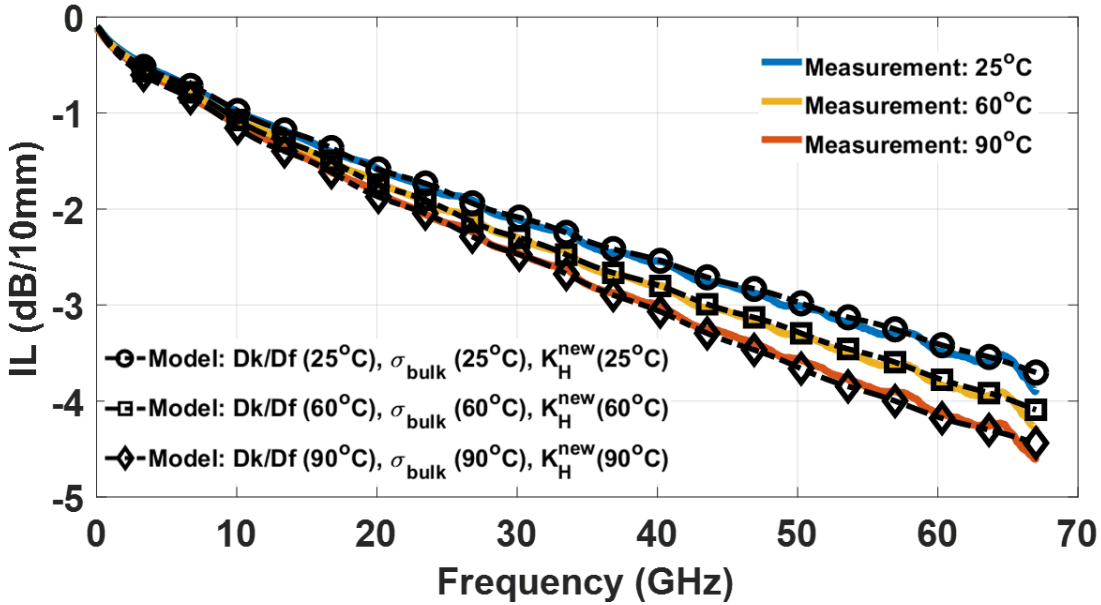


C. S. Geyik, Y. S. Mekonnen, Z. Zhang and K. Aygün, "Impact of Use Conditions on Dielectric and Conductor Material Models for High-Speed Package Interconnects," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 10, pp. 1942-1951, Oct. 2019

- Capturing impact of environmental conditions requires a temperature and humidity dependent modeling and characterization flow

Impact of Environmental Conditions





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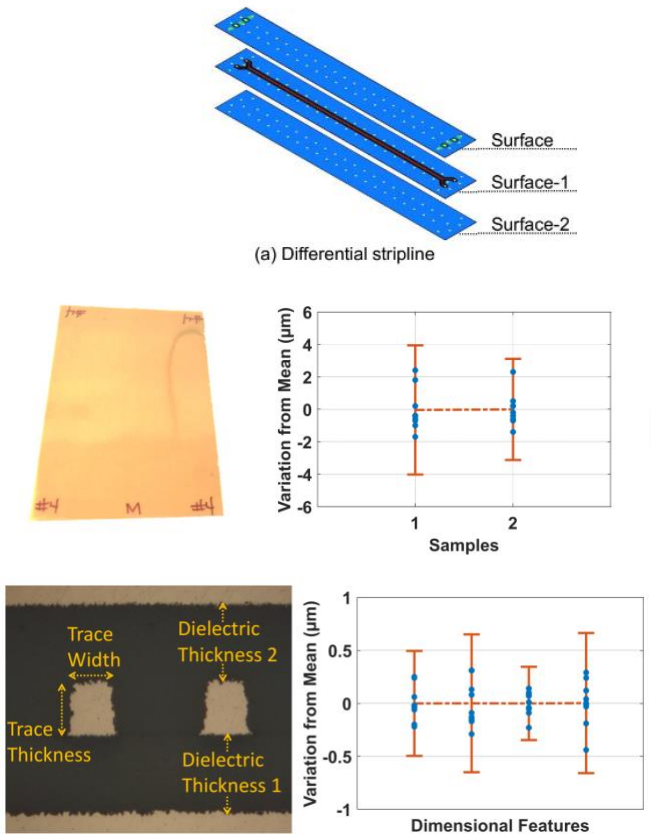
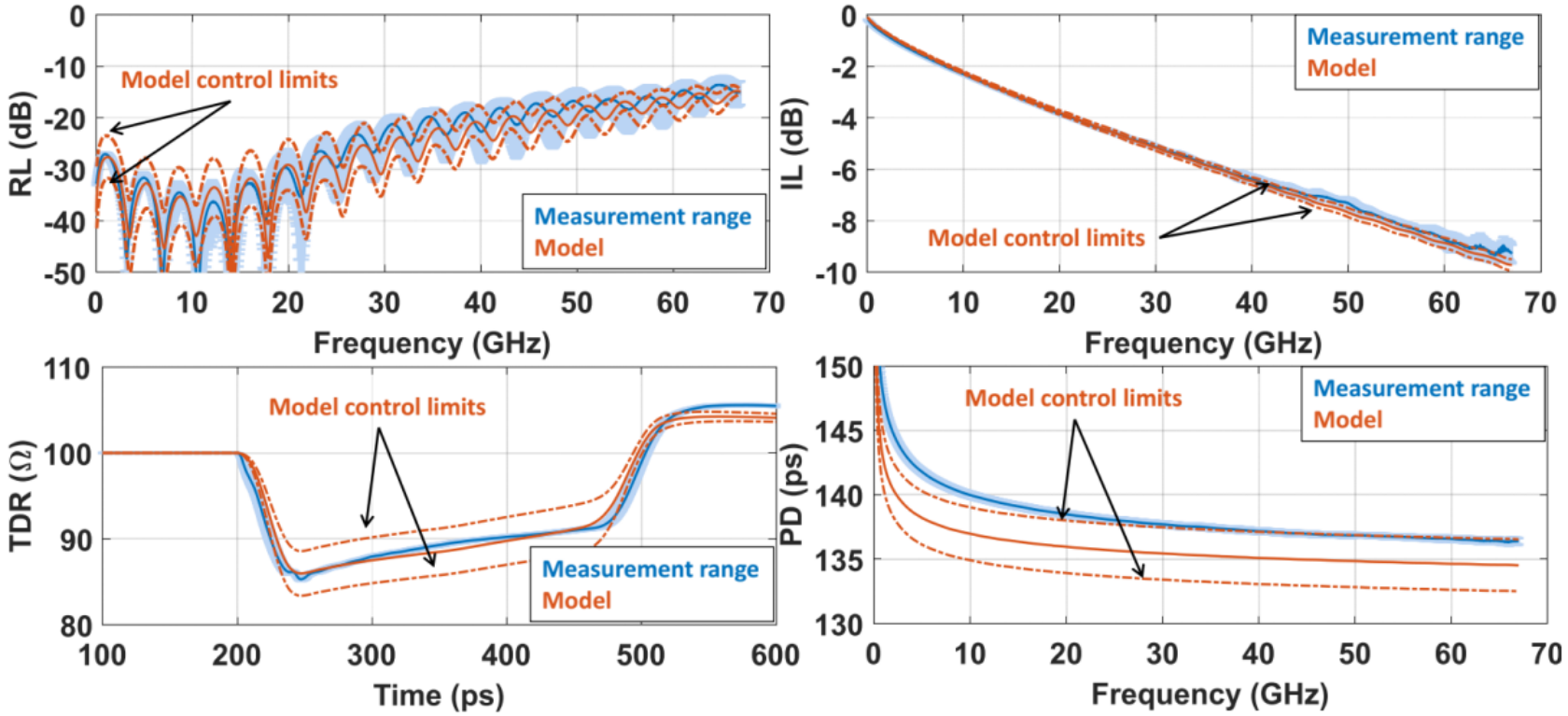
$$K_H^{\text{new}}(T,\delta,sr,a) = 1+\frac{3}{2}sr\left(1+\frac{\delta}{a}+\frac{\delta^2}{2a^2}\right)^{-1}+c_1(T-T_0)e^{-c_2\delta}$$

- Temperature dependent material properties and surface roughness models help further improve measurement to modeling correlation quality

Impact of Measurement Uncertainties



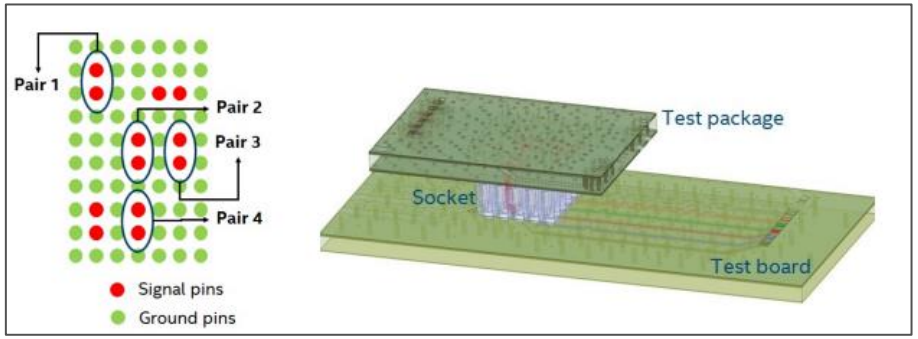


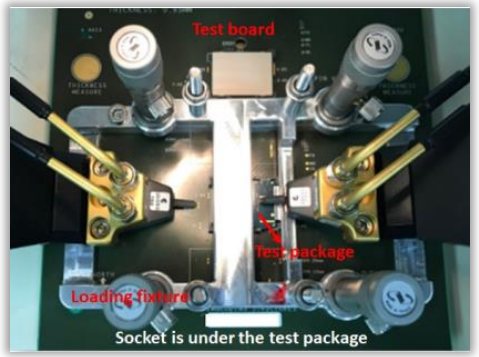
C. S. Geyik, M. J. Hill, Z. Zhang, K. Aygün and J. T. Aberle, "Measurement Uncertainty Propagation in the Validation of High-Speed Interconnects," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3

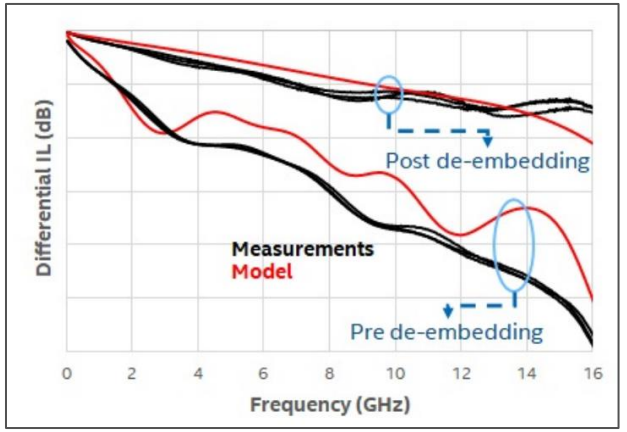
- Generating high-fidelity package electrical models requires precise modeling & measurement methods, environmental control, and understanding of uncertainties for each measurement

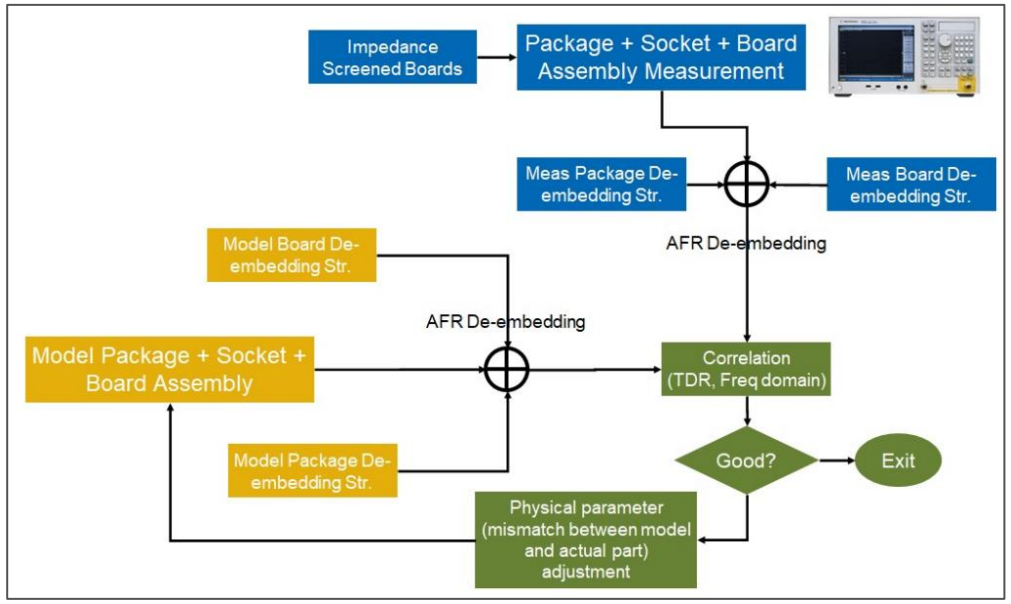
Accurate HSS Modeling of Package/PCB Interface: Socket

Land grid array socket

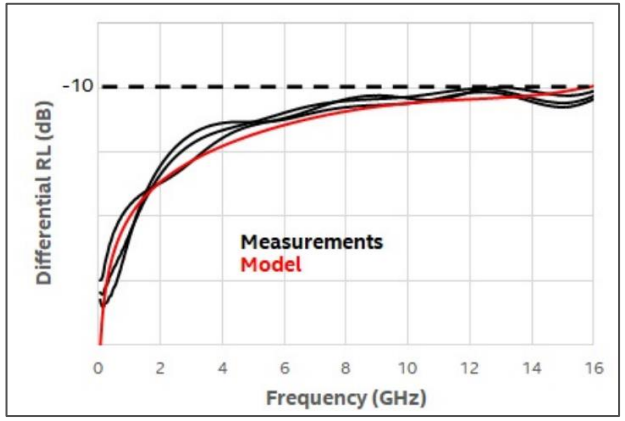


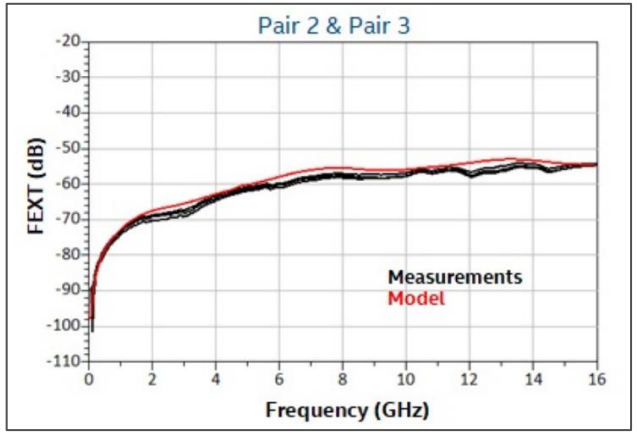






Proposed methodology for socket measurement-to-modeling correlation

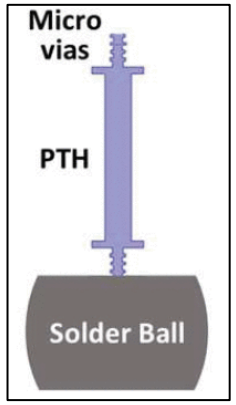


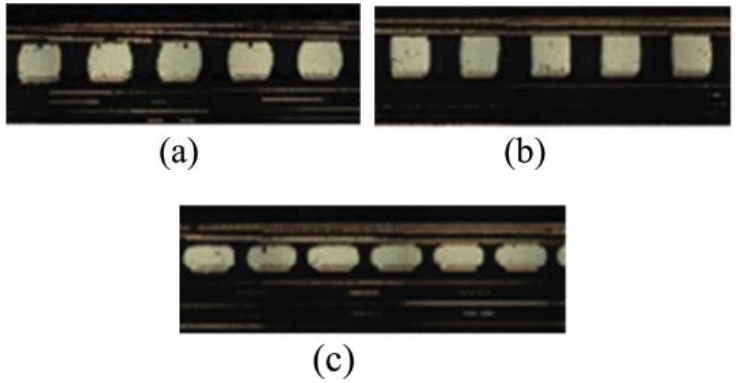


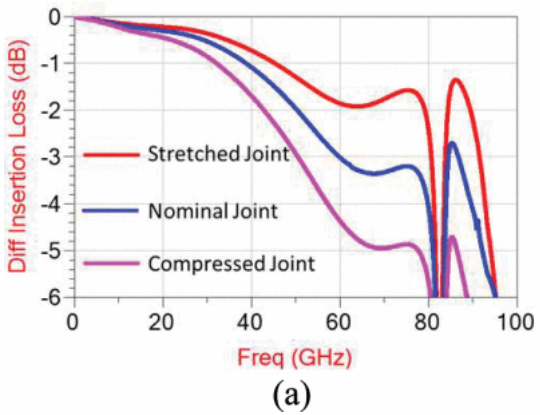
S. Mondal, D. Athreya, E. Davies-Venn, Z. Zhang and K. Aygün, "An Improved Methodology for High Frequency Socket Performance Characterization," 2022 IEEE 31st Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2022, pp. 1-3

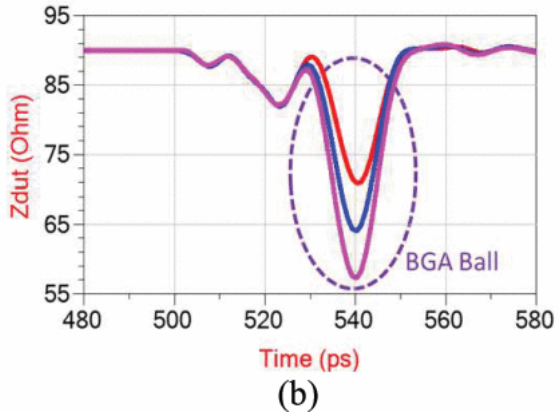
- Accurate HSS modeling of Package/PCB Interface is critical to develop technology solutions for SERDES HSS

Accurate HSS Modeling of Package/PCB Interface: BGA



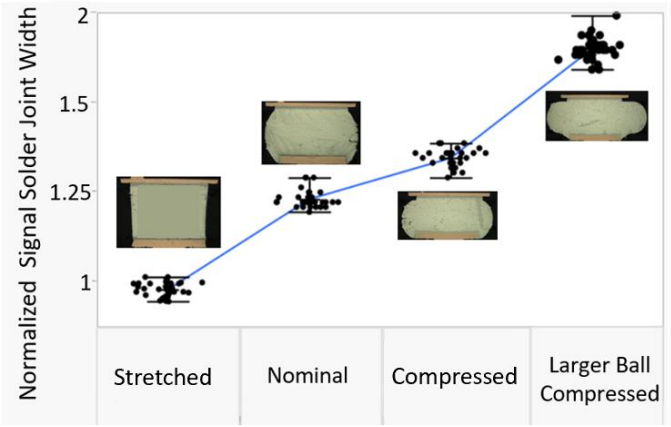


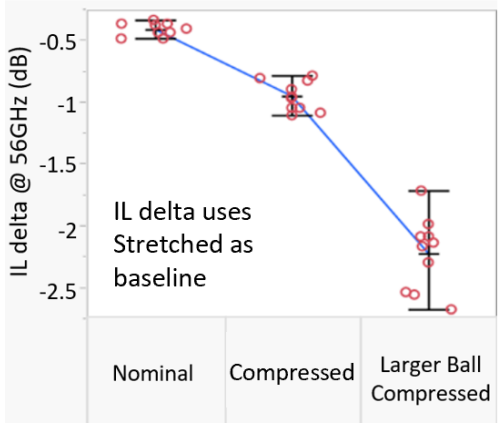




J. Sun, Z. Qian, C. S. Geyik and K. Aygün, "Accurate BGA Package Solder Joint Modeling for High Speed SerDes Interfaces," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3

Measured impact of BGA shape in insertion loss



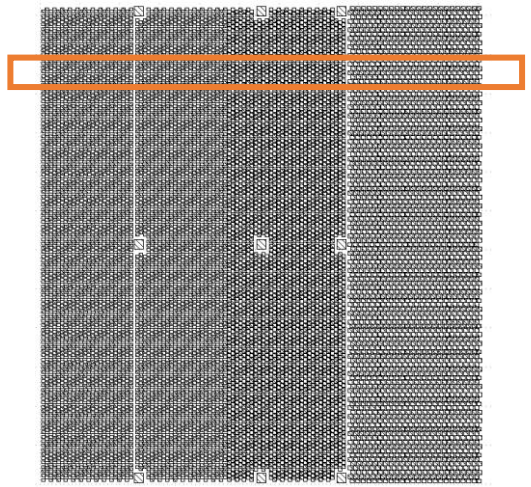


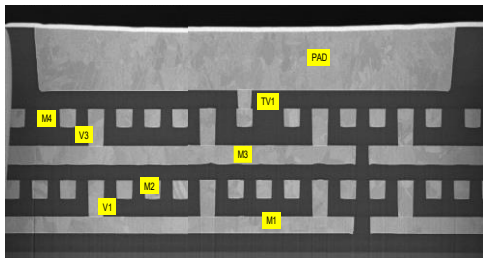
More details at IEEE EPEPS 2023

- Accurate HSS modeling of Package/PCB Interface is critical to develop technology solutions for SERDES HSS

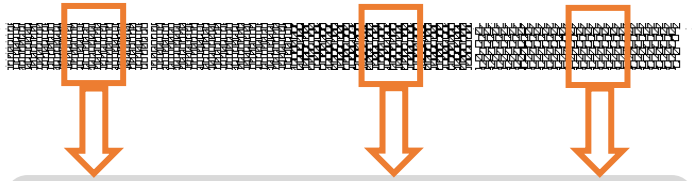
Accurate HSS Modeling for 2.5D Packages

Full Bridge Die





Repeating Block



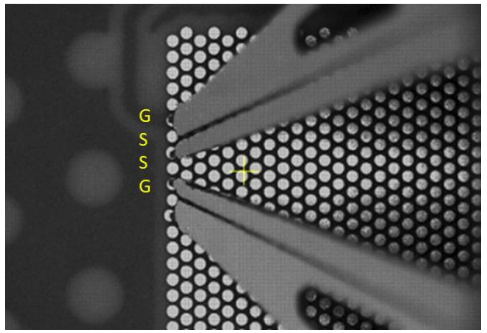
3D Full-wave Solver

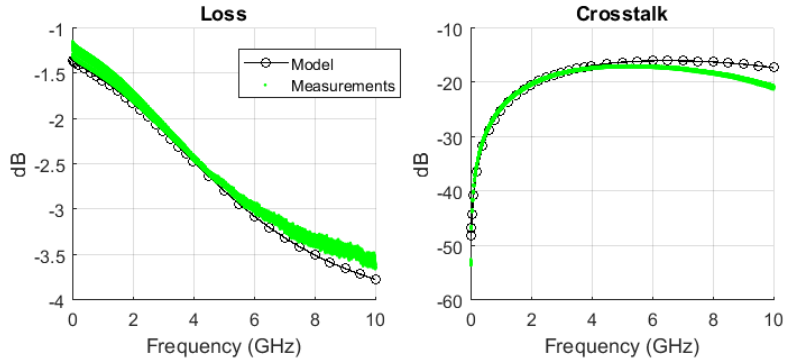
S-param → tabular RLGC*

Length Scalable Channel Assembly

* *Y. Chu, J. Yu, and Z. Qian, "Robust and efficient RLGC extraction for transmission line structures with periodic three-dimensional geometries," IEEE EMC&SI 2015*

Probing on Substrate Surface





Z. Qian, J. Xie and K. Aygün, "Electrical Analysis of EMIB Packages," 2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2018

- Extra fine features in 2.5D packages require new interconnect modeling methodologies

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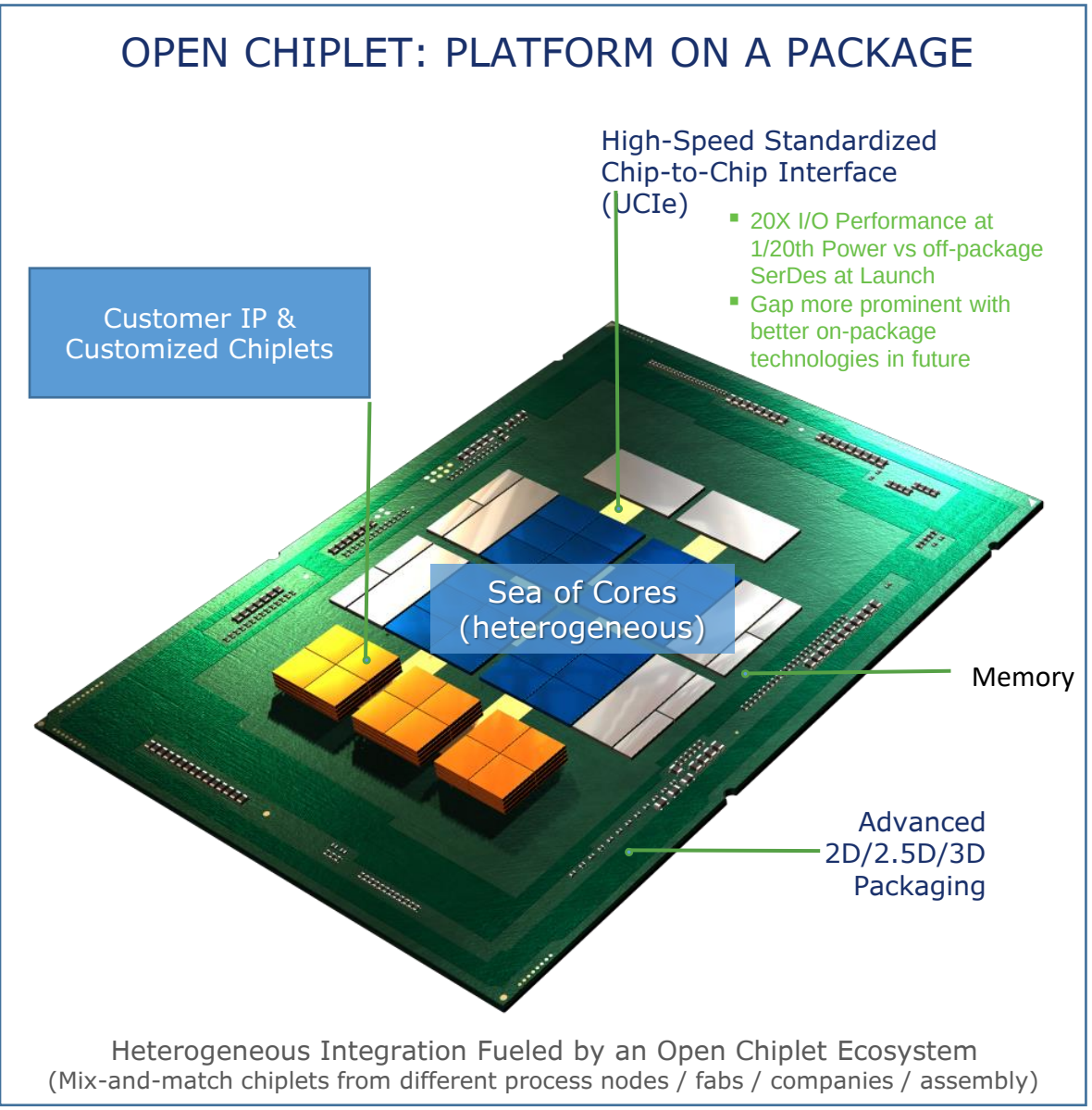
Motivation

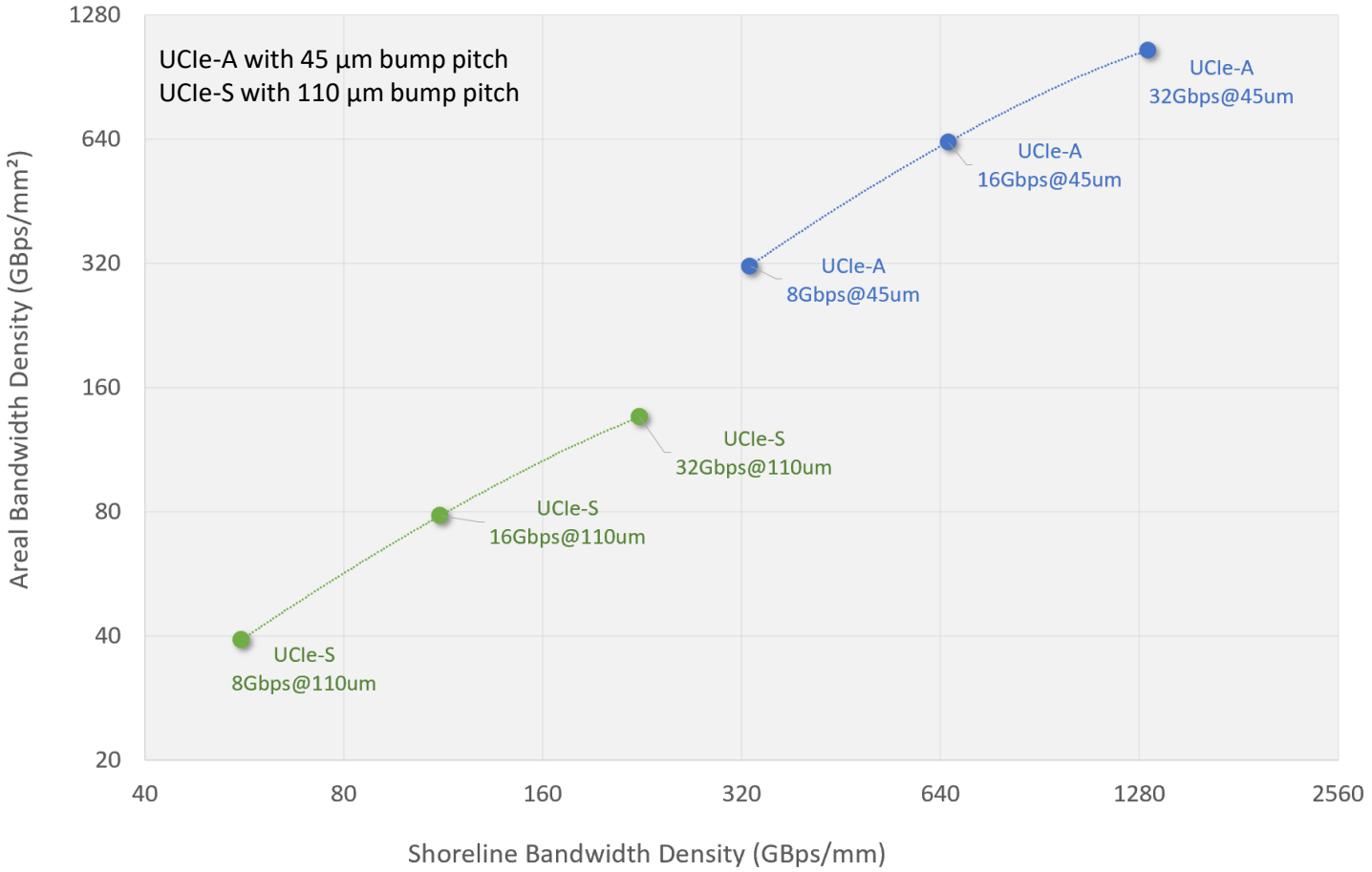


Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)

D. D. Sharma, Universal chiplet interconnect express (UCIe)®: Building an open chiplet ecosystem, Beaverton, OR, USA, Mar. 2022 (available at uciexpress.org).

Bandwidth Performance Target of UCIe



IEEE Heterogeneous Integration Roadmap

Generation Number[10] →		1	2	3	4	5
Raw Linear Bandwidth Density (GBps/mm)[11,12,13]		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	50	40	35	30
	Linear Escape Density (IO/mm)[14]	500	667	1000	1500	2000
	Areal Escape Density (IO/mm²)	331	400	625	816	1111
Signaling Speed (Gbps)[15]		2	3	4	5.33	8

Table 4: Physical IO Scaling Roadmap 2D and Enhanced-2D Architectures that use Solder based Interconnects

Generation Number →		1	2	3	4	5
Raw Linear Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)[16]	55	40	30	20	10
	Linear Escape Density (IO/mm)	500	667	1000	2000	4000
	Areal Escape Density (IO/mm²)	331	625	1111	2500	10000
Signaling Speed (Gbps)		2	3	4	4	4

Table 5: Physical IO Scaling Roadmap for 2D and Enhanced-2D Architectures that use both solder and hybrid interconnects

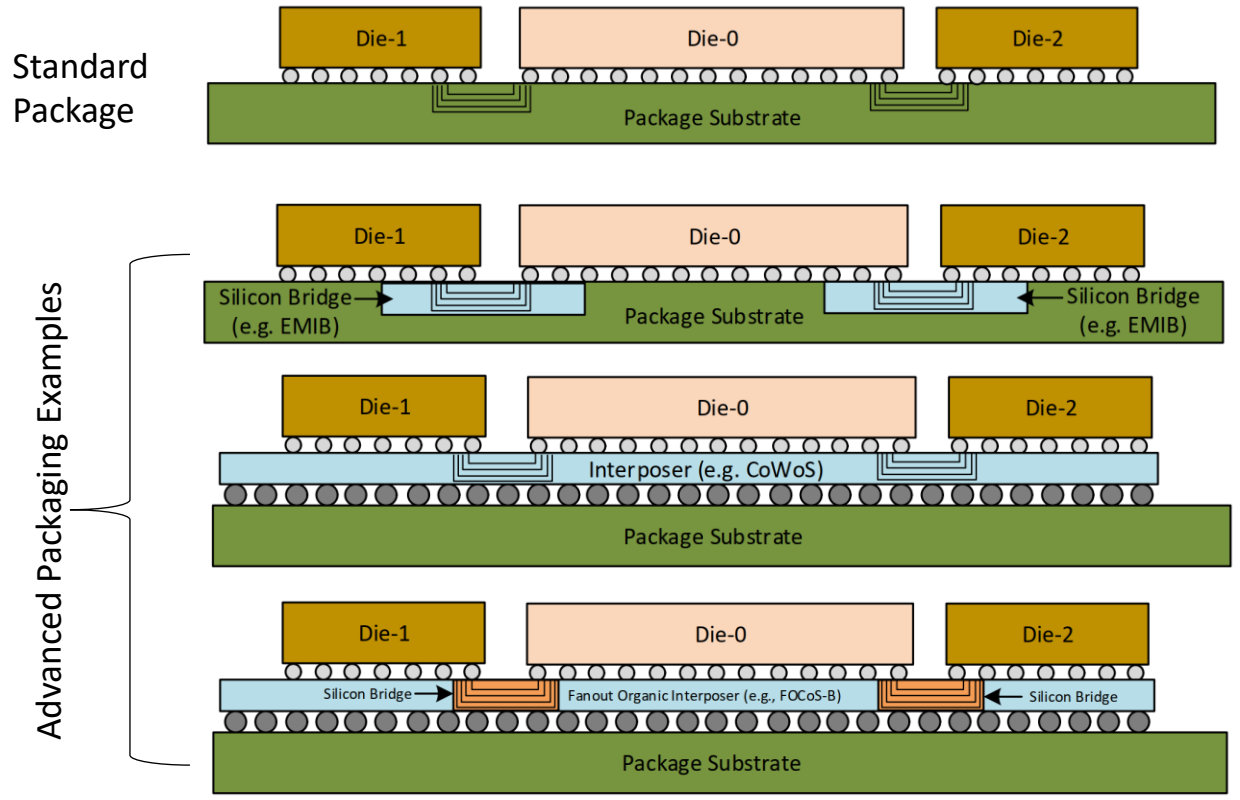
UCIe 1.0: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

Significant bandwidth density scaling via standard and advanced packaging

Packaging Technologies supported by UCIe



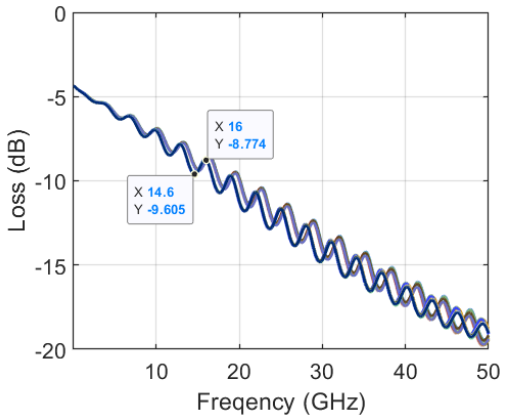
UCIe supports various packaging technologies

D. Das Sharma, G. Pasdast, Z. Qian and K. Aygun, "Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 9, pp. 1423-1431, Sept. 2022.

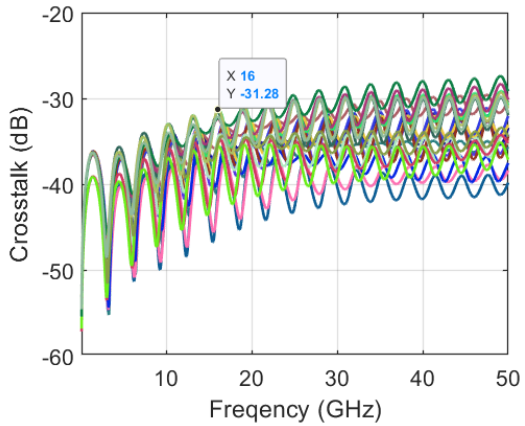
Reference Standard & Advanced Channel Solutions

25mm length

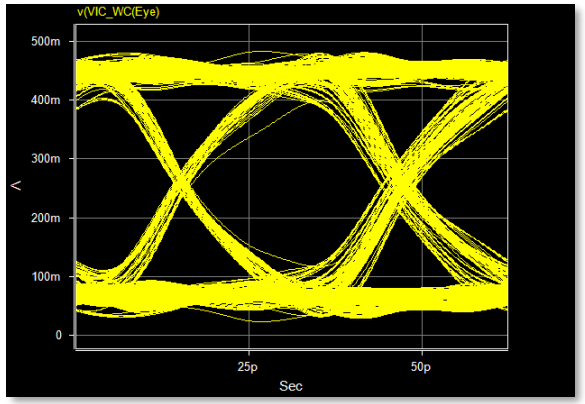
VTF Loss



Cumulative VTF Crosstalk

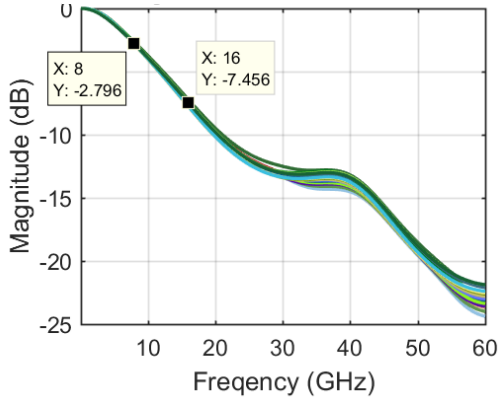


32Gb/s Eye Diagram

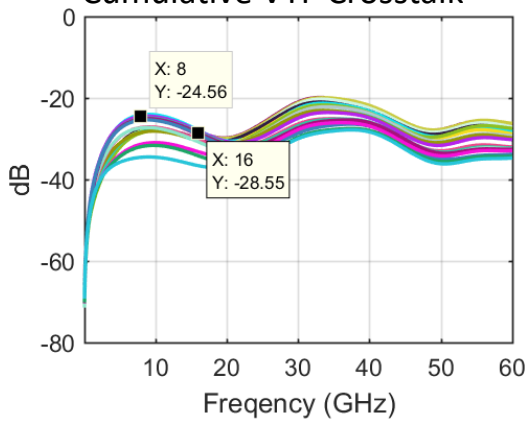


A 224 GB/s/mm organic channel UCIe-S solution is demonstrated

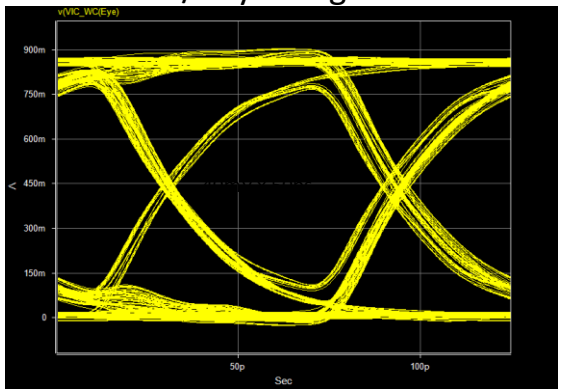
VTF Loss



Cumulative VTF Crosstalk



16 Gb/s Eye Diagram



A 658 GB/s/mm EMIB channel UCIe-A solution is demonstrated

D. Das Sharma, G. Pasdast, Z. Qian and K. Aygun, "Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 9, pp. 1423-1431, Sept. 2022.

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IEEE EPS Conferences

http://www.epeps.org/

https://www.linkedin.com/groups/86343/

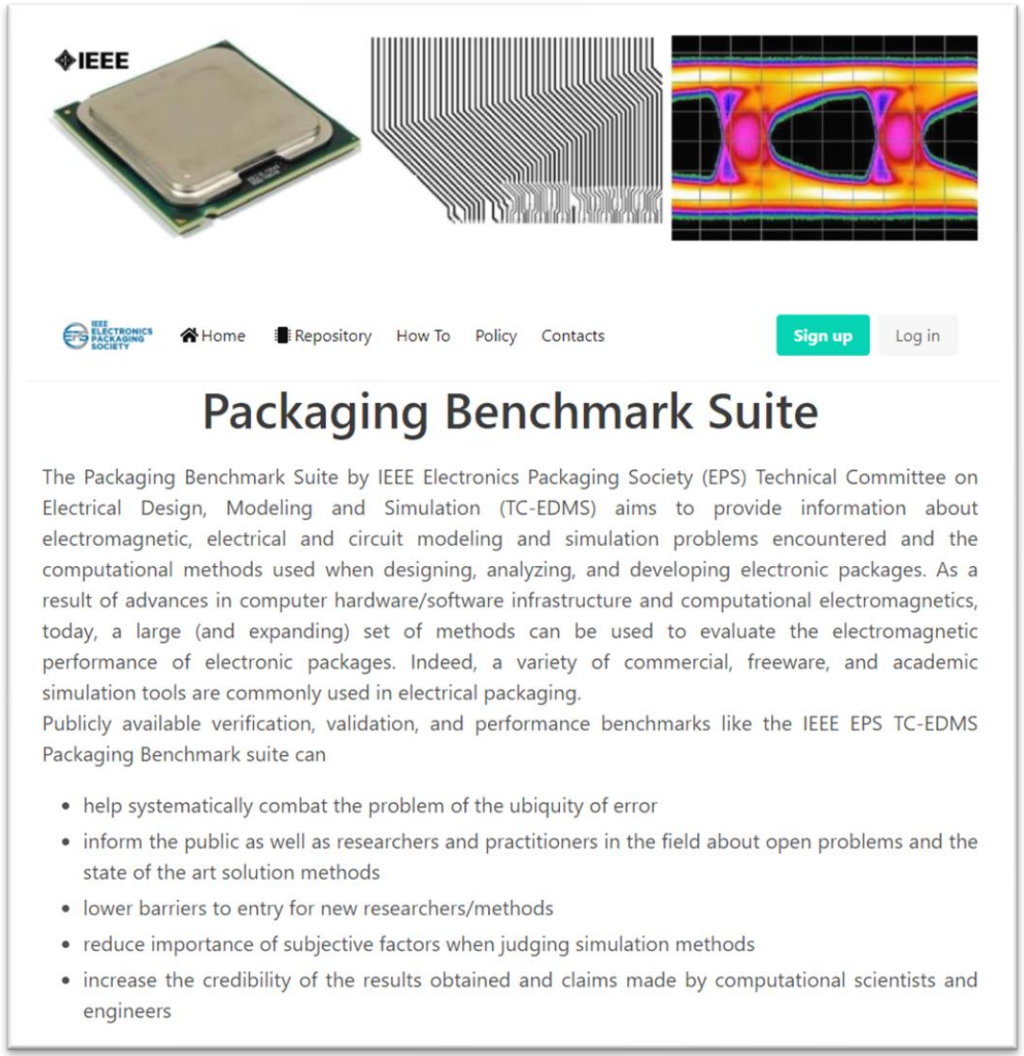
https://spi2024.av.it.pt/

http://www.edaps.org/

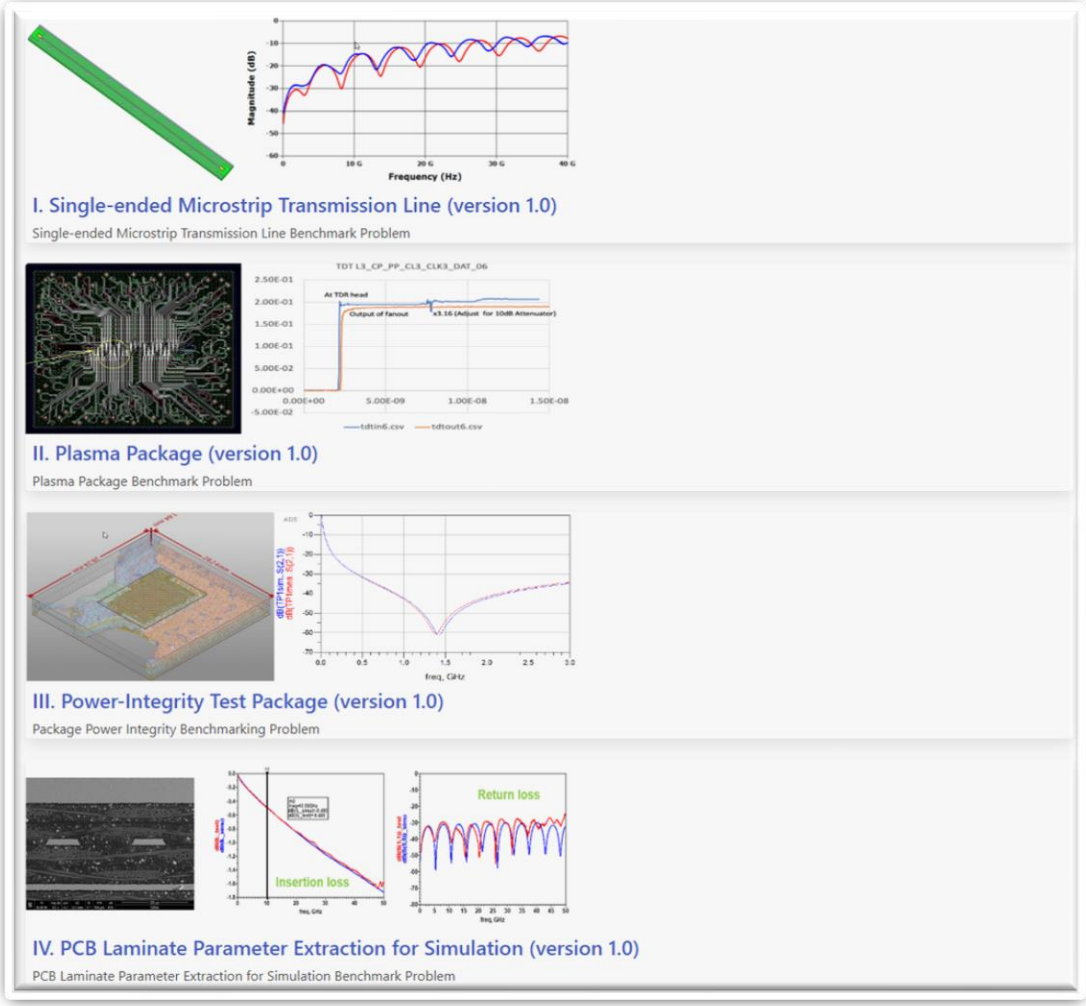
https://www.ectc.net/

- Multiple IEEE EPS conferences focused on electrical analysis of packaging and systems

IEEE EPS TC-EDMS Packaging Benchmarking Suite



https://packagingbenchmarks.org/



- Benchmark problems helping the research community to develop new methods and tools

Summary

- Semiconductor packaging is experiencing an accelerated pace of innovation fueled by emerging electronic system connectivity and heterogeneous integration demands
- Novel advanced packaging architectures provide new opportunities to improve high-speed signaling for short reach interconnects
- These new technologies need to include features to enable also high-speed signaling for off-package long reach interconnects
- Validated modeling methodologies & collaterals are key for both existing and emerging package and system designs
- Emerging standards such UCIe are helping the industry with further acceleration of adoption of heterogenous integration architectures