Heterogeneous System Component Integration with Nanopackaging

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Heterogeneous Integration with Nanopackaging

• Nanopackaging for Power:
  • Capacitors, Inductors, 3D integration

• Nanopackaging for RF:
  • Passives, FSS, Tunable Elements
  • Antennas
  • Integrated heat-spreaders
  • EMI shields

• Nanopackaging for Wearable:
  • Additively-deposited Nanowire-nanoparticle interconnects
  • Wireless power + capacitive storage

• Nanopackaging for Neuro:
  • Electrodes, hermetic coatings, power sources, wireless power
Vision: Convert 2D PCBs to 3D chip-scale Modules

Power Electronics
- GaN and SiC – Low-cost Fan-Out Packaging
- Power conversion and regulation with PMIC, inductors and capacitors

RF and mm wave Packaging:
- Reconfigurable RF packages
- 3D antenna-in-packages

3D Chiplet-Scale Modules

Wireless neural recording:
- Antenna, mixer or Diode with matching networks
- Multiferroic Power/data telemetry;
- Chiplets with telemetry, rectifier and storage elements

Wireless photonic sensors:
- LED, Diodes, Amplifiers Drivers, power sources with 3D interconnections

P M Raj, John Volakis and Shubhendu Bhardwaj
Wafers to Systems – Past, Present and Future

From 1990s

- Dicing
- Discrete Packaged IC
- Laptop

From 2000s

- Packaging
- Wafer-Level Packaged IC
- High-performance computing

From 2010s

- Dicing
- Fan-Out Packaged IC
- Smartphone

From 2020s

- 3D Package Integration
- Textiles/Wearables

- I/Os 100-1000 Mobile processors
Nanopackaging Drives Future Hardware

- **Power**: Nanocapctors and inductors
- **Thermal**: Cu-Graphene heat-spreaders
- **Reliability**: ALD Inorganic films
- **Humidity barriers**: Nanodielectrics and additive interconnects for 5G and wireless sensors
- **RF**: Electrodes
- **Bioelectronics**: Power and data telemetry
- **Remateable connectors**: Storage capacitors

[Diagram showing interconnections of components]

https://ieeenano.org/nanopackaging-tc
Minimize the stages of power conversion;

Perform power conversion right near the load;

Figures from EPC (Alex Lidow) and IBM Zurich (Arvind Sridhar)

Utilize Advances in:
- GaN
- CMOS integration
- Topologies
- Passive components
Need for Embedded Power Passives

SMT Discrete Inductors
- Low efficiency
- High profile
- Large footprint

Discrete Inductors
- Higher efficiency
- Granular power supply for each IC designs
- Miniaturized modules
- Short PDN path: Reduce the need for decoupling
- Reduce impedance

Substrate embedded passives
- Low profile
- Small footprint

PCB

Interconnection Length

Module Thickness

Component Density
## R&D Needs

<table>
<thead>
<tr>
<th>Capacitors</th>
<th>Density</th>
<th>High K dielectrics; Enhance electrode surface area; New dielectrics and deposition processes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Frequency stability</td>
<td>Electrodes and connectivity with lower parasitics</td>
</tr>
<tr>
<td></td>
<td>Integration</td>
<td>Thinner form-factors; Substrate or wafer or fan-out embedding</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Inductors</th>
<th>Density</th>
<th>Higher permeability with saturation field and high resistivity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Efficiency</td>
<td>Low coil DC losses; Low core losses with low coercivity and eddy currents</td>
</tr>
<tr>
<td></td>
<td>Integration</td>
<td>Substrate- or wafer-compatible process</td>
</tr>
<tr>
<td></td>
<td>Current-handling</td>
<td>Design innovations; Scalability in thickness to handle higher current</td>
</tr>
</tbody>
</table>
## Magnetic Material Options Today

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness Microns</th>
<th>Coercivity A/m</th>
<th>Resistivity ( \mu ) Ohm cm</th>
<th>Saturation Flux (Tesla)</th>
<th>Permeability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mn,Zn ferrites</td>
<td>&gt;100</td>
<td>3-5</td>
<td>10,000</td>
<td>0.6</td>
<td>5000</td>
</tr>
<tr>
<td>Nanocrystalline and amorphous flakes</td>
<td>&gt;15</td>
<td>3</td>
<td>110</td>
<td>1.2</td>
<td>15000</td>
</tr>
<tr>
<td>Electroless thinfilms</td>
<td>3-5</td>
<td>10-20</td>
<td>100</td>
<td>1</td>
<td>&lt;&lt;1000</td>
</tr>
<tr>
<td>Plated thin films</td>
<td>2-100</td>
<td>20-80</td>
<td>35</td>
<td>1.3</td>
<td>~1000</td>
</tr>
<tr>
<td>Flake composites</td>
<td>25-500</td>
<td>100-200</td>
<td>10,000</td>
<td>0.8</td>
<td>100-150</td>
</tr>
<tr>
<td>Nanomagnetic films</td>
<td>1-10</td>
<td>10</td>
<td>200-300</td>
<td>1.5</td>
<td>200-500</td>
</tr>
</tbody>
</table>

### 0.1 – 5 MHz

### 1 – 10 MHz

### 10 – 150 MHz
# Inductor Technologies

<table>
<thead>
<tr>
<th></th>
<th>Discrete (Ferrite or Metal powder)</th>
<th>Magnetic composites –substrate-embedding</th>
<th>Nanomagnetic films: On-chip</th>
<th>Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/Rdc nH/milhohm</td>
<td>15-25</td>
<td>5-10</td>
<td>0.1-0.2</td>
<td>&gt;&gt;10</td>
</tr>
<tr>
<td>Q</td>
<td>&gt;20</td>
<td>&lt;10</td>
<td>5</td>
<td>&gt;20</td>
</tr>
<tr>
<td>Current-handling A/mm²</td>
<td>0.01 – 0.1</td>
<td>0.1 – 1</td>
<td>5-10 A/mm²</td>
<td>5-10 A/mm²</td>
</tr>
<tr>
<td>Thickness</td>
<td>200-500 microns</td>
<td>50 - 200 microns</td>
<td>25 microns</td>
<td></td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

Discrete (Ex. 0.5 x 0.1 x 0.5 mm)

KEMET-Tokin

Nitto Denko

Substrate-embedded inductors Magnetic Core (0.5 - 0.6 mm)

Intel and Ferric
High-Density Embedded Inductors for Integrated Voltage Regulators (Carlos Riera Cercado, Huy Nguyen)

**Objectives**

• Embedded inductors for power converters:

  Target
  20 nH/milliohm
  2 A/mm²
  20-50 microns

**Unique Approach**

1. Substrate-compatible magnetic composites with high permeability
   • High permeability for high-inductance density
2. Embedded solenoid inductors
   • Embedding for miniaturization
   • Design for high-current density
3. Substrate design rules to fabricate thick copper
   • Low resistance

**Prior Art**

**Major Accomplishments**

• Embedding of high current density and high-efficiency inductors embedded in organic substrates. Current status:
  • Thickness: 500 μm
  • Inductance: 8nH/mm²
  • Current: Projected to 1 A/mm²
  • Resistance: projected to <10 m Ω

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1. Substrate-
2. Compatible magnetic composites with high permeability
3. Embedded solenoid inductors
4. Substrate design rules to fabricate thick copper
5. Dielectrics
6. Copper winding
7. Magnetic cores
8. IC
9. Substrate
10. Magnetics
11. substrate
# Capacitor Technologies

<table>
<thead>
<tr>
<th></th>
<th>MLCC (Murata)</th>
<th>Trench Caps (Murata)</th>
<th>Ta Chip (AVX)</th>
<th>Emerging Need</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Volumetric Density</strong></td>
<td>20 µF/mm³</td>
<td>1 µF/mm³</td>
<td>~10 µF/mm³</td>
<td>50-100 µF/mm³</td>
</tr>
<tr>
<td><strong>Thickness</strong></td>
<td>100 µm</td>
<td>100 µm</td>
<td>600 µm</td>
<td>50-100 µm</td>
</tr>
<tr>
<td><strong>Freq. Stability</strong></td>
<td>10-100 MHz</td>
<td>&gt;1-10 MHz</td>
<td>0.2 -1 MHz</td>
<td>&gt;10 MHz</td>
</tr>
<tr>
<td><strong>ESR</strong></td>
<td>~10 mΩ</td>
<td>50 mΩ x µF</td>
<td>&gt;100 mΩ x µF</td>
<td>~50 mΩ x µF</td>
</tr>
<tr>
<td><strong>% ΔC/V</strong></td>
<td>-13 % to -70% (1 to 4 V)</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
</tr>
<tr>
<td><strong>Max. Temp</strong></td>
<td>85°C</td>
<td>150°C</td>
<td>125°C</td>
<td>&gt;125°C</td>
</tr>
</tbody>
</table>

PICK AND PLACE

FILM EMBEDDING
WAFER OR PANEL INTERCONNECTS
High-Density Capacitors for Integrated Voltage Regulators

**Objectives**

- Ultra-high density capacitors:
  - >1 \( \mu \text{F/mm}^2 \) at 1 MHz, 3-48 V, & 50 m\( \Omega \) ESR
  - 1 n\( \text{A/\mu F} \) leakage current
  - Simpler processing on wafer or package
  - 100 \( \mu \text{m} \) thickness
  - >105°C stability

**Unique Approach**

- Printed Tantalum Nanoparticles Anode
  - High-surface area at ultra-thin form-factor
  - Scalable to any design need
- Nanoscale \( \text{Ta}_2\text{O}_5 \) Dielectric
  - Paraelectric for DC bias and temperature stability
  - Amorphous for low leakage current
- Conformal Conducting Polymer Cathode
  - Low-resistivity and thick coating for low ESR
  - Self-healing for low leakage current
- Foil-transfer integration
  - Thin-film lamination
  - Ultra-short copper interconnections for reduced impedance
  - Low-cost, panel-scale, 3D approach

**Prior Art**

<table>
<thead>
<tr>
<th></th>
<th>MLCC</th>
<th>Trench Caps</th>
<th>Ta Chip</th>
<th>Emerging Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric Density</td>
<td>20 ( \mu \text{F/mm}^3 )</td>
<td>1 ( \mu \text{F/mm}^3 )</td>
<td>~10 ( \mu \text{F/mm}^3 )</td>
<td>50-100 ( \mu \text{F/mm}^3 )</td>
</tr>
<tr>
<td>Thickness</td>
<td>100 ( \mu \text{m} )</td>
<td>100 ( \mu \text{m} )</td>
<td>600 ( \mu \text{m} )</td>
<td>50-100 ( \mu \text{m} )</td>
</tr>
<tr>
<td>Freq. Stability</td>
<td>10-100 MHz</td>
<td>&gt;1-10 MHz</td>
<td>0.2-1 MHz</td>
<td>&gt;1 MHz</td>
</tr>
<tr>
<td>ESR</td>
<td>~10 ( m\Omega )</td>
<td>50 ( m\Omega \times \mu \text{F} )</td>
<td>&gt;100 ( m\Omega \times \mu \text{F} )</td>
<td>~50 ( m\Omega \times \mu \text{F} )</td>
</tr>
<tr>
<td>% AC/V</td>
<td>-13 % to -70% (1 to 4 V)</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
</tr>
<tr>
<td>Max. Temp</td>
<td>85°C</td>
<td>150°C</td>
<td>125°C</td>
<td>&gt;125°C</td>
</tr>
</tbody>
</table>

**Major Accomplishments**

- >1\( \mu \text{F/mm}^2 \) up to 1 MHz at 5 V with low ESR, low leakage current, and 100 \( \mu \text{m} \) component thickness
Embedded Capacitors Roadmap

Board or package embedding; I/O decoupling; 100 MHz

Embedded polymer laminate and dielectrics
- 0.1 nF/mm² Polymer laminate dielectrics
- 0.5 nF/mm² Polymer film dielectrics
- 1 nF/mm²

Embedded ceramic film
- 2-3 nF/mm² Thin oxides
- 20-30 nF/mm² BaTiO₃ film
- 30-50 nF/mm² enabled by new multicomponent oxides

Wafer-integrated capacitors
- 0.08 µF/mm²
- 0.25 µF/mm²
- 0.5 µF/mm²
- Silicon capacitors Deep trench
- Ultra-high surface area silicon 1-2 µF/mm²
- Multilayered dielectrics on deep trench

IVR; Embedded PoL 1-20 MHz

Package embedding; Core and I/O decoupling; 100-500 MHz

Embedded capacitors Panel
- Adv. Nanotech. >3 µF/mm²
3D Power Packaging

- Multiphysics converter design (topology & hardware co-design)
- Advanced GaN devices & high-temp passives

Infineon

- Structure and process innovations
- Doubleside wafer plating
- Panel-scale embedding of power devices
- High-temperature materials with enhanced interfaces for Hi-Rel

Schweizer

- Sintered copper interconnections between devices, IMS or leadframe and PCB
- Barriers for oxygen and moisture
- Advanced encapsulants

ASE

AT&S

- Advanced cooling loop with temp uniformity
- System-level thermomechanical and electrical reliability:
## Evolution of Die-Attach Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Pressureless assembly capability</th>
<th>Electrical and thermomechanical reliability performance</th>
<th>Safety</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-lead solders</td>
<td>Pressureless</td>
<td>Moderate with low homologous temperature</td>
<td>Lead-based</td>
<td>High</td>
</tr>
<tr>
<td>Transient Liquid Phase Sintering</td>
<td>Requires pressure</td>
<td>Moderate with kirkendall voids</td>
<td></td>
<td>Moderate</td>
</tr>
<tr>
<td>Nanosilver</td>
<td>Requires more pressure</td>
<td>Microstructural instabilities and diffusion</td>
<td></td>
<td>Low, because of design and process flexibility</td>
</tr>
<tr>
<td>Nanocopper</td>
<td>Pressureless with reactive nanosurfaces</td>
<td>Die shear strength is low with smooth backside metallization</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nanocopper-microwire-graphene multilayers</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Koduri, Texas Instruments (Current is not needed for lateral GaN die-attach)*

*Infineon*  
*Jiang Li (TI, Virginia Tech)*  
*Vanessa Smet, Georgia Tech*
Heterogeneous 5G System Integration

- RF and digital in the same package
- High-density and low-loss transmission lines:
- Ultra-fine vias and TPVs for seamless 3D interconnects
- Precision circuitry for impedance matching
- Smooth surface for low losses
- Package- and board-level reliability
- Large-area panel processing

- Advanced antenna array for wideband and gain
- Embedded FSS for improved performance
  - Heterogeneous high-K superstrates as lenses, E walls, H walls, AMCs

FSS Heterogeneous High K dielectrics
Antennas with Nanoscale Magnetodielectrics

- Size is proportional to \( \frac{1}{\sqrt{\varepsilon_r \mu_r}} \)
- Bandwidth improves with impedance match with air:
  - \( \mu_r \sim \varepsilon_r \)
  - High \( \mu \), Low loss tangents
- Radiation Efficiency
- Permeability of 2-2.5
- Permittivity of 6-12
- Combined effect reduces size by 80%
- Increases bandwidth by 10X
- Efficiency remains almost same

Traditional antenna

Nanomagnetic antenna

Magneto-dielectric

\( \mu_r \mu_0, \varepsilon_r \varepsilon_0 \)

Standard FR-4

Patch Antenna
Tunable BSTs can eliminate the PCM switch assembly, interconnect lengths and losses

Cobalt Nanowire NonReciprocal Components (Circulators, Isolators)

High-K mm wave Superparaelectrics for AMCs
Tong-Hong Lin, GT

Cu (AMC pattern)

Laminated Glass

Cu (Reflector)

Tunable Nanoscale Superparaelectrics for Beamforming and band rejection
Alwan, Volakis et al., FIU

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Table: Size Reduction Rate

<table>
<thead>
<tr>
<th>Unit-cell size (mm)</th>
<th>Operational Band (GHz)</th>
<th>FBW (%)</th>
<th>Size Reduction Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without BST</td>
<td>2.42</td>
<td>24.5 ~ 30.4</td>
<td>21.5</td>
</tr>
<tr>
<td>0.6 μm BST</td>
<td>2.24</td>
<td>24.3 ~ 29.8</td>
<td>20.3</td>
</tr>
<tr>
<td>3 μm BST</td>
<td>1.7</td>
<td>24 ~ 29.8</td>
<td>21.6</td>
</tr>
<tr>
<td>Ceramic-Polymer + Glass</td>
<td>1.5</td>
<td>24.4 ~ 30.2</td>
<td>21.3</td>
</tr>
<tr>
<td>Ceramic-Polymer Composite</td>
<td>1.16</td>
<td>24.5 ~ 30</td>
<td>20.2</td>
</tr>
</tbody>
</table>
Multiferroic Tunable Shields and Filters for Secure RF Electronics

- Multiferroic based electromagnetic architectures for smart shielding.
- Planar EM substrate architectures for smart substrates (with tunable permittivity) for antennas.
- Frequency selectivity and direction selectivity for EM blocking.

Bhardwaj, Venkatakrishnan, FIU
Nanopackaging for 6G and THz
Hybrid front-end for dynamic all-spectrum sensing and communication in 6G

6G System-on-Package

Graphene-based THz radiation sources

Precision THz antenna arrays
(ex. 1024 elements in 1 mm²) and Phase shifters

Lenses and intelligent metasurfaces with space-time-frequency coding

Low-loss interconnects and waveguides

High-responsivity low-noise detectors to surmount the high path-loss at these frequencies

Muhammad Ali, GT
Bioelectronics: Why 3D heterogeneous integration:

- Reduce footprint and volume:
  - Vertical integration of power, signal and stimulation functions

- Functionalizing the electrode tip:
  - Chiplets (thin chips) close to the electrode array

- Band-aid patch-like smart sensors and therapies
  - Integrate antennas, RF ICs and electrode arrays
  - Passive neural recording with RF in and out

- Integrate power sources:
  - Tiny telemetry link
  - Tiny flexible conformal capacitors

- Vertical remateable area-array connectors:

- Reduce reliability issues:

Argus Retinal Prosthetics

Smart catheters with rolled fan-out flex packages

Multielectrode arrays from IPGs (FDA approved for human subjects)

Neural Dust for brain-computer interfaces

Courtesy: Argus Retinal prosthetic system 2013, Ranu Jung and Anil Thota,
Christine Kallmayer, Fraunhofer IZM
Dongjin Seo, UC Berkleay
Bioelectronic Packaging Focus at FIU

- Hermetic feedthroughs with remateable interfaces
- Nearfield telemetry
- Wireless neural recording
- Neuroelectrodes
- 3D package integration

- Simplified analog front-end topologies for stimulation and sensing
- High-density charge storage and delivery
  - (capacitors 10-100 microfarad/mm³)
- Hermetic feedthroughs
- High wireless power transfer efficiency:
  - >80% with separation of 10 cm with metamaterials
- Remateable area-array microcontacts
- Analog/RF Passives
- Dielectric
- Ground
Electronics in Flex – Flex in Textiles

Program Vision and Impact

*All wearable electronics are integrated with textiles

Electronic platform for multimodal sensing.
Objectives:
Neural recording:
  Wearable on-skin patches
  Implantable for Peripheral Nervous System
Sensitivity of < 30 microvolts
Communication with smartphone

Approach:
RF backscattering technique
Completely-passive: zero-power:
  No active circuits that need voltage bias
Miniaturized antennas with advanced designs

Innovative Packaging:
Design and Integration with physiological inputs
Chip-on-flex or chip-in-flex fan-out packaging
Embedded-chip for
Low –impedance skin or implantable electrodes

Advanced antennas:
  • Dual-band monopole antenna
  • Miniaturized patch antenna with high-K
Low-loss flex-compatible interconnects
  • <0.1 dB end-to-end loss
Graphene – PEDOT-PSS electrodes for high-fidelity low-impedance recording

Smallest zero-power wireless neural recording system:
Dual-band antenna
Embedded or backside IC assembly
Thin flex package (100 microns)
Chiplet integration (100 microns)

P M Raj, John Volakis and Shubhendu Bhardwaj
Flex-Textile Hybrid Packaging (Abdal Abdulhameed, Monir Monshi)

1) Packaging of low-power batteryless extraction circuits
   - Simplify the on-site electronics,
2) Highly planar and unobtrusive integration of RF comm./data interfaces with textiles,
3) Remateable (reconnectable) flex interconnections to modularize sensing electronics and for replacing biofouling parts
4) Integrate with point-of-care centers for eventual diagnosis by practitioners, while ensuring privacy and data security.

Thermomechanical modeling of flex and textile-embedded packages under flexion

- Lower chip-to-flex Interconnect stresses
- Lower flex-to-textile stresses

Conductive elastomer adhesives

Fluroelastomer encapsulation

Stable resistance under thermal and humidity testing

P M Raj, John Volakis and Shubhendu Bhardwaj
Remateable Connectors Packaging (Jose Solis Camara, Sepehr Soroushiani)

- Remateable flex-to-flex and flex-to-textile Packages
  - End-user or manufacturer can remove and re-assemble
- Examples of use:
  - Power harvesting and RF communication
  - Sensor and communication interfaces
  - Fine pitch and area-array
  - Low-cost additive manufacturing

Initial remateability demonstrated with multiple bending cycles, assembly and re-assembly

Via-Filling and Interconnect Layer Assembly

- Via-fill of metal-elastomer nanocomposites in elastomer polymer films;
- Can be scaled down to 200 micron pitch

Screw clamps are used for the first demonstration;

Push-button or micro-Velcro assembles are currently investigated

P M Raj, John Volakis and Shubhendu Bhardwaj
Hermetic Packaging: Feedthroughs and Remateable Area-Array Connectors

Karbasi, Jones, FIU

Cofired ceramic and Pt
85 micron vias
332 feedthroughs in 7 mm
Area-array Pt bonding with sintered Pt nanoink

LCP with metal feedthroughs
(Pd-coated copper)
75 micron vias
Sundaram, GT-PRC

https://www.integer.net/

Sepehr Soroushiani, FIU
3D Wireless Power Delivery and Capacitive Storage

Magnetic flux concentration or metamaterials for better power transfer efficiency

Efficiency (%)

Frequency (MHz)

Capacitance (μF/mm²)

Frequency (MHz)

Mahmoud Sharafi, FIU

Grant Spurney, GT
Implanted Electrodes

- Biocompatibility
- Charge injection: >5 mC/cm²
- Low impedance: < 0.1 ohms x cm²
- Mechanical tissue compatibility

Boretius, Biosens. Bioelec 2010

Fattahi, Advanced Materials, 2014

Redrawn from data reported in Kosteralos, Advanced Materials 2018.

Kelly Rojas, FIU
Summary

• Heterogeneous package integration for future systems

• Power Modules:
  • Passive components with high storage densities; 3D packaging
  • Diamond-like heat-spreaders; low thermal impedance bonding interfaces

• RF:
  • Nanodielectrics and nanomagnetic films for passives, antennas
  • Nanowire arrays for circulators, isolators
  • THz array – integration of sources, detectors with antenna arrays and waveguides

• Bioelectronics:
  • Electrode arrays with pulse generators or recording units
  • High-efficiency power and date telemetry
  • Zero-power data telemetry
  • Remateable interfaces