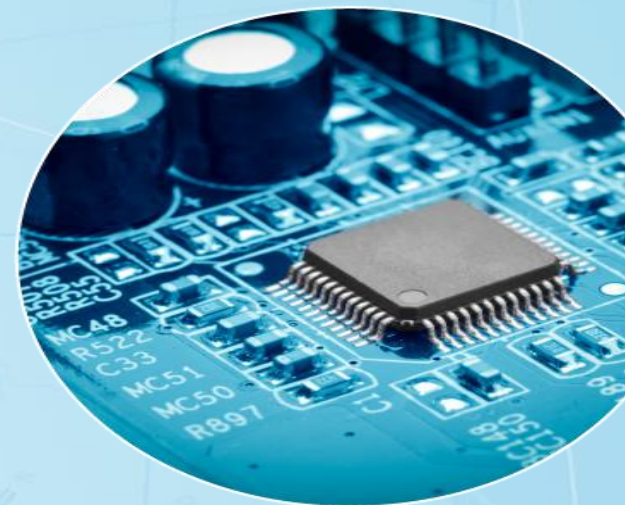




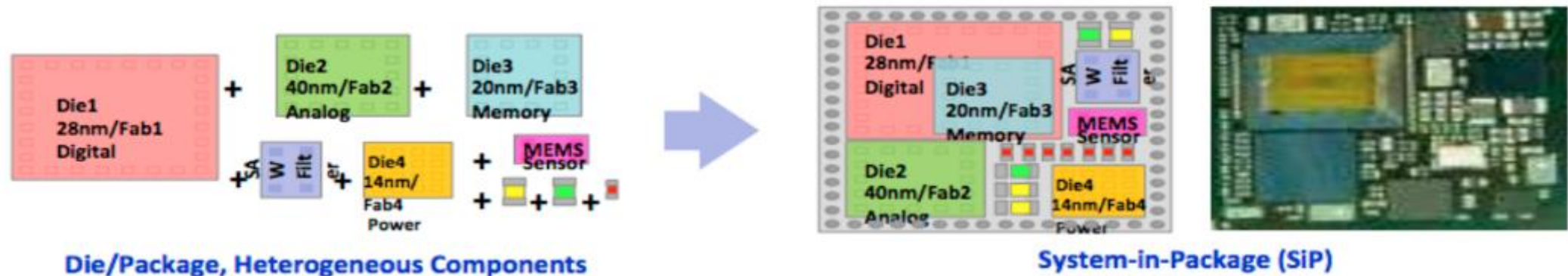
Short Introduction to the goals of HIR Modelling mission

Chris Bailey
EPS, President
Co-Chair – M&S Chapter



Heterogeneous Integration Defined

Heterogeneous Integration refers to the integration of separately manufactured components into a higher level assembly (SiP) that, in the aggregate, provides enhanced functionality and improved characteristics



- Integration: Different nodes, MEMS, Si Photonics, Power ICs, etc
- Miniaturised by Advanced Packaging (SiP Toolbox)
- Performance optimised - Signal and power integrity
- Decrease development time & Improved reliability
- Flexible, re-usable & re-configurable design

Heterogeneous Integration Roadmap

Topic/Theme	Technical Working Group
Heterogeneous Integration Components	Single-Chip and Multi-Chip Packaging (includes Substrates)
	Integrated Photonics (includes Plamonics)
	Integrated Power Devices
	MEMS
	RF and Analogue Mixed Signal
Cross-Cutting Topics	Emerging Research Materials
	Emerging Research Devices
	Interconnect
	Test
Integration Processes	SiP
	3D & 2.5D
	WLP (fan-in & fan-out)
Packaging for Specialised Applications	Mobile
	IoT and Wearable
	Automotive
	High Performance Computing
Design	Co-Design, Modelling and Simulation
Supply Chain	Elements of the Supply Chain Appropriate for Pre-Competitive Collaboration

ITRS:
1991 - 2015

- Precompetitive
- 15 years outlook & 25 years for emerging materials & devices
- Sponsored by five global semiconductor associations. Appoint IRC & approve governance
- Volunteer driven
- Free access
- CMOS "Moore's Law" node driven
- 17 Technical Working Groups

HIR:
2016 --

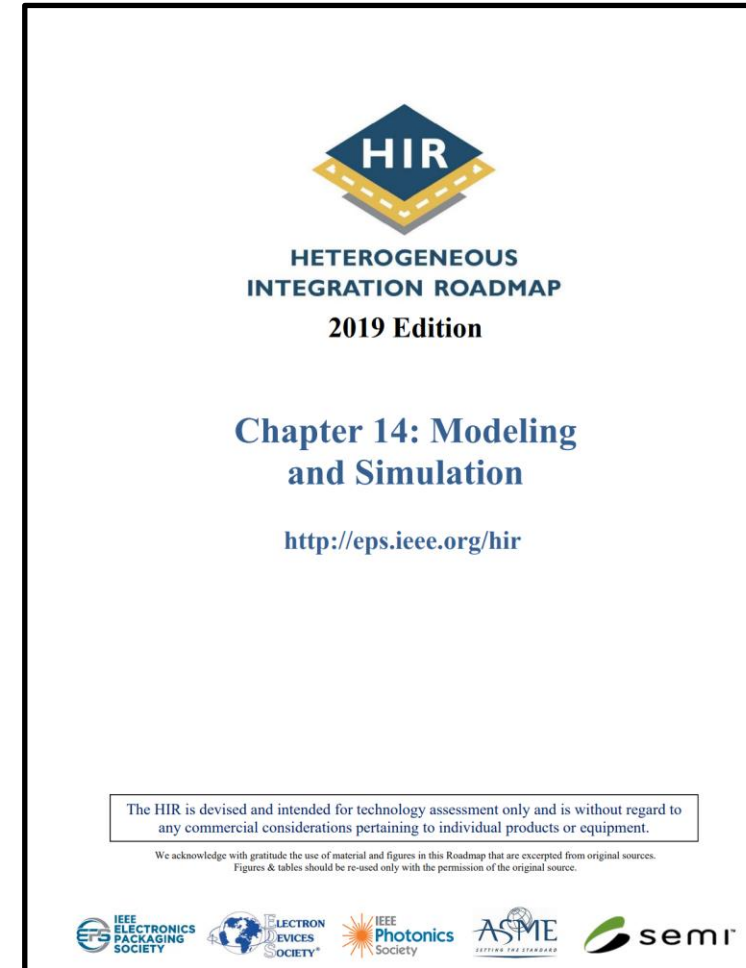
- Precompetitive
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- Volunteer driven
- Free access
- Systems & application driven
- 19 Technical Working Groups



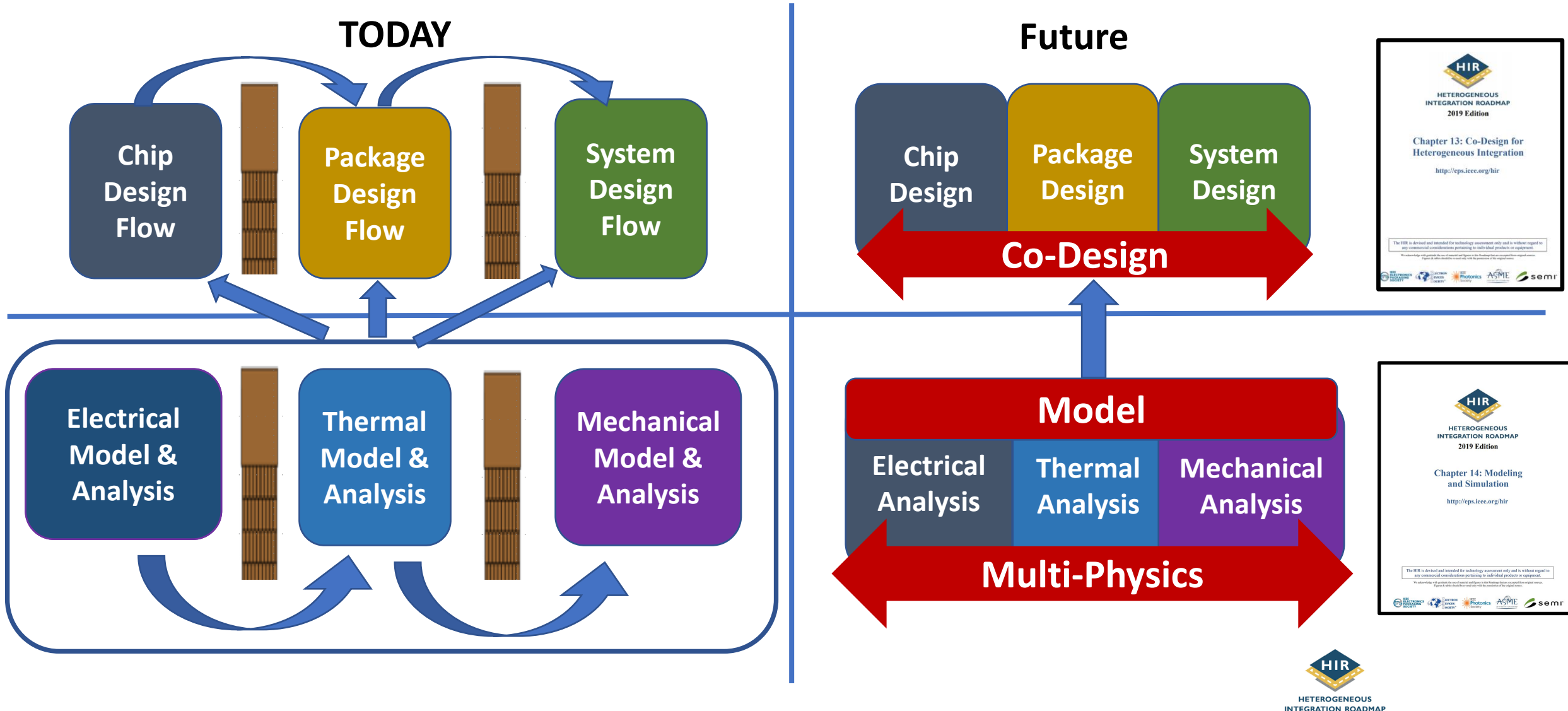
<https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html>

Scope

- Five sections
 - Electrical Analysis
 - Thermal Analysis
 - Materials Modelling & Process Models
 - Mechanical & Multi-Physics Analysis
 - Reliability and Prognostics
- Chapter details
 - State of the Art & Challenges
 - Potential solutions

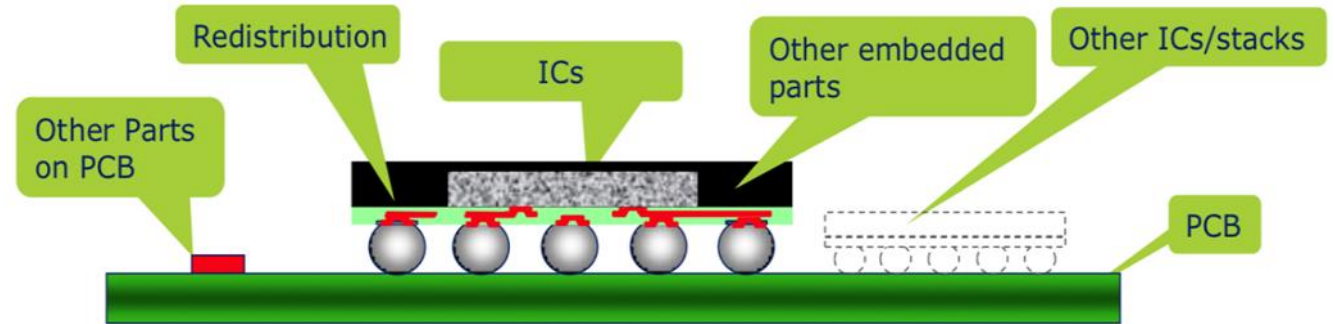


Moving towards a new paradigm



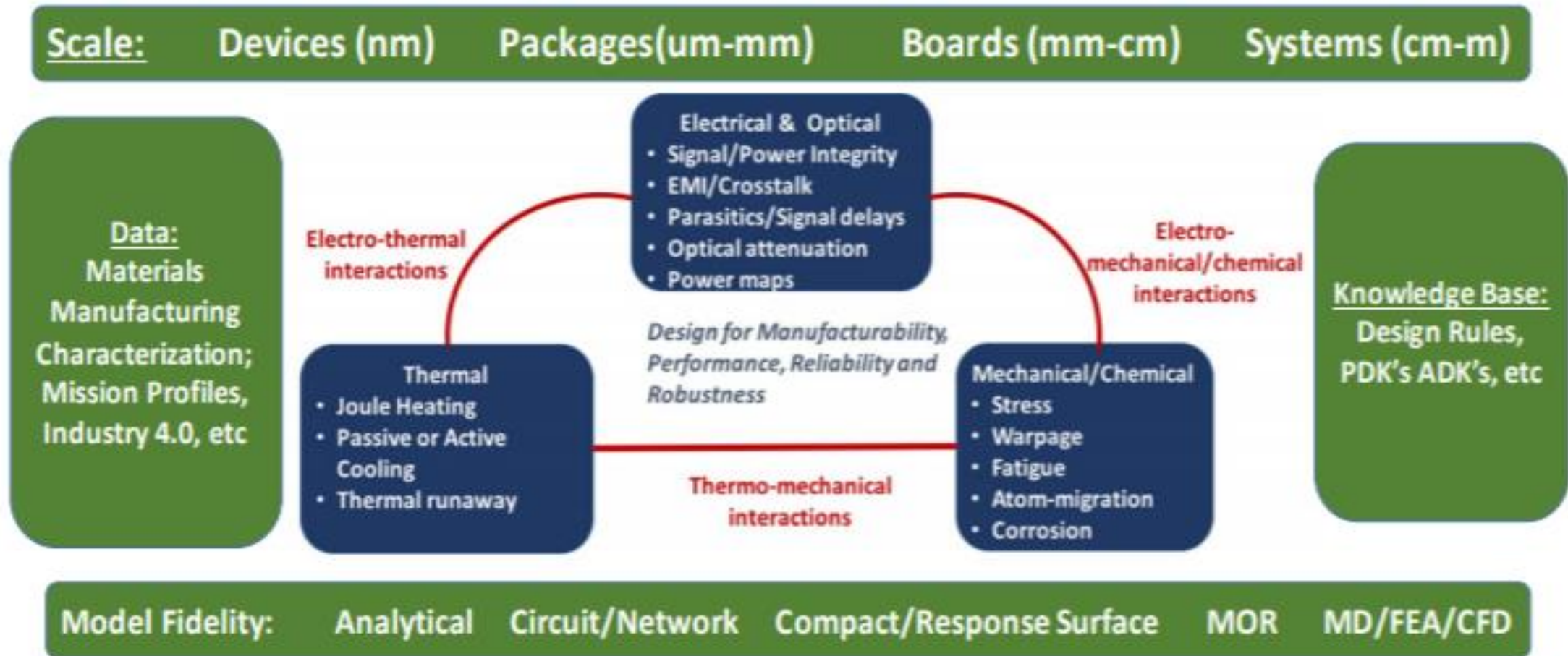
Co-Design Requirements

- Design Challenges:



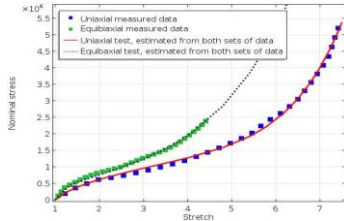
- Many technologies within one project
 - Different Si tech's – substrate/RDL – PCB – other components
 - Multiple length scales
 - Interdependencies: dies, package, test, and board
 - Independent optimization at different levels does not lead to optimize system
- Need global optimization (chip – package – board/system)
 - Higher performance, reduced cost, better quality and reliability

Modelling & Simulation

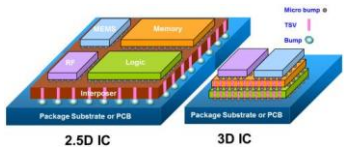


Physics of Failure (PoF) Based Reliability Modeling

Material Properties



Design Information



Application Conditions



Stochastic Process Modelling

Physics of Failure

Electronic
Simulation

Optical
Simulation

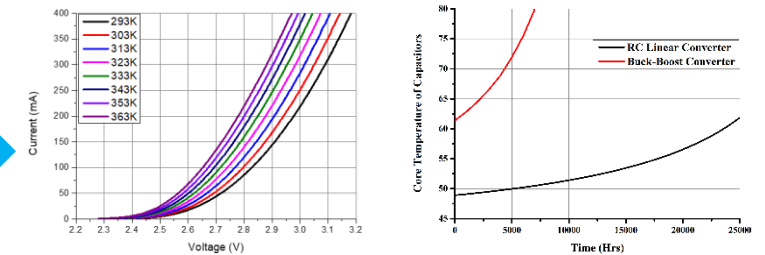
Thermal
Simulation

Failure or Degradation

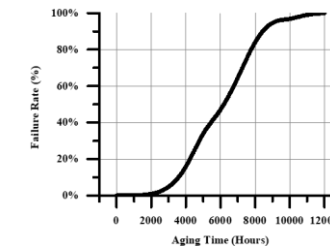
Temperature/time dependent Failure or Degradation

Monte Carlo Simulation

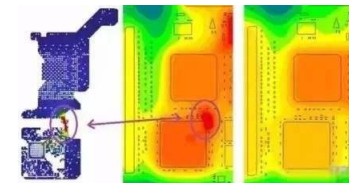
History of Electronic-Thermal Behavior



Reliability/ Lifetime/ MTTF



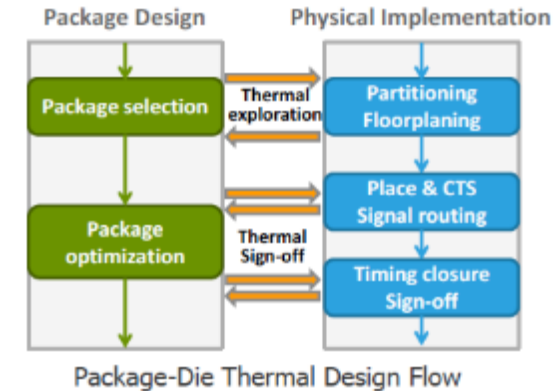
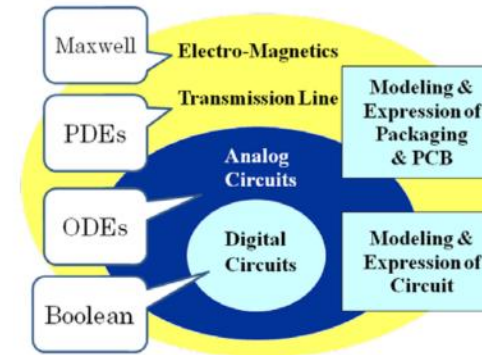
Critical Component & Material



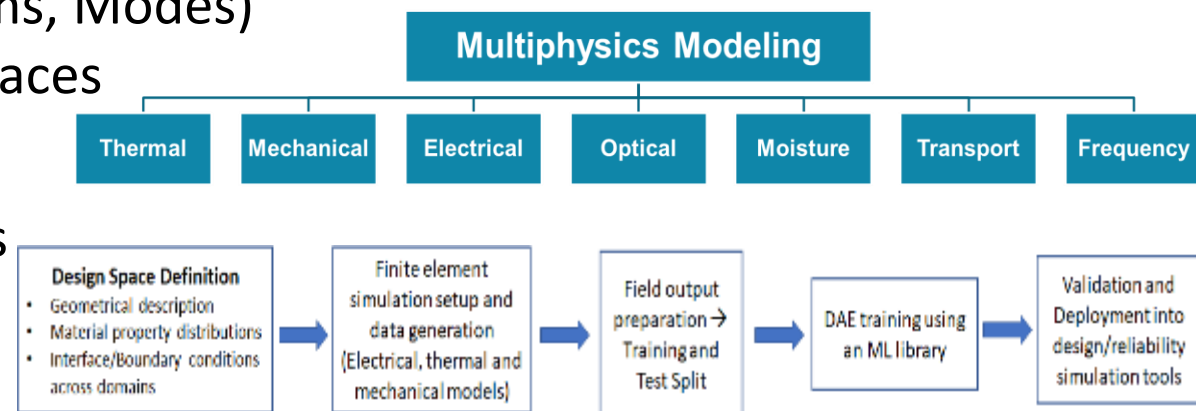
B. Sun, X.J. Fan, et al., RELIABILITY ENGINEERING & SYSTEM, 2017;
B. Sun, X.J. Fan, et al., IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, 2016;

Highlights from 2019 Edition of HIR

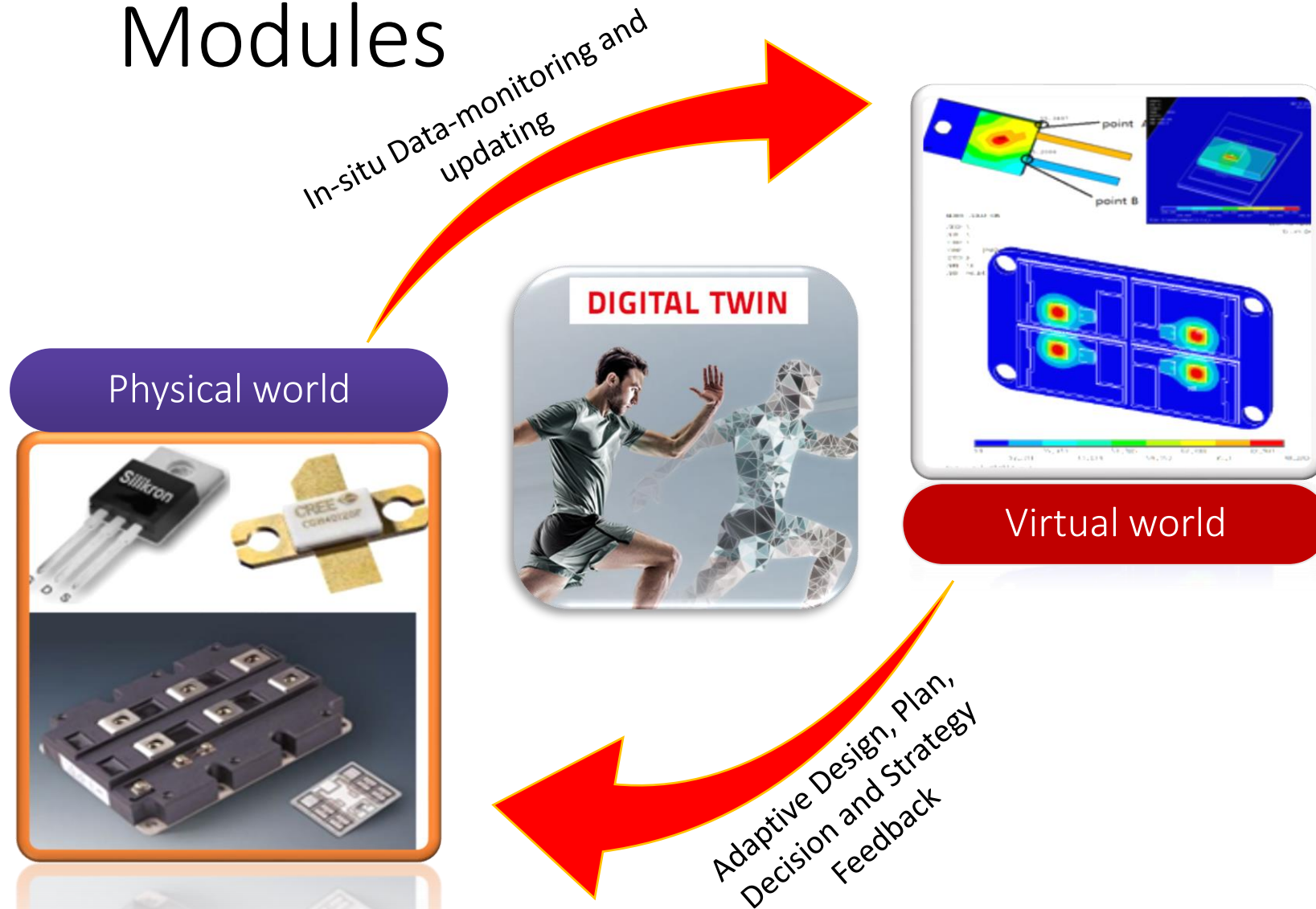
- State of the art
 - FEA, CFD, FDTD ... Compact Models, Spice
 - EDA Tools ... Spreadsheets
- Examples of Challenges
 - Electrical - Simulate across features (within die and die-die coupling)
 - Electro-Thermal – Predicting hot spots (Joule Heating, Thermal Runaway)
 - Electro-Thermal-Mechanical – Stress on transistors (Mobility shifts)
 - Reliability – Physics of failure (Mechanisms, Modes)
 - Materials – Stochastic behaviour & interfaces
- Potential solutions
 - Multi-physics/scale modelling techniques
 - Model order reduction techniques
 - Machine Learning & AI



DAC Designer Track 2017 | *Pascal Vivet*



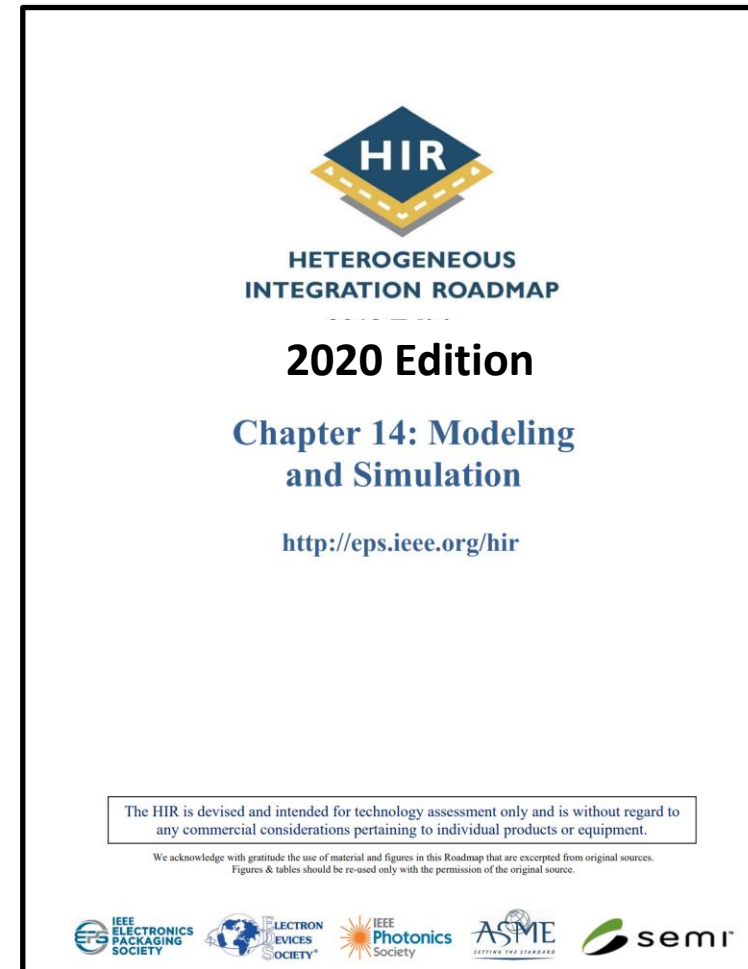
Digital Twin for Electronic Components and Modules



- Digital Twin is the ultimate aim of product design, reliability and lifetime management.
- Modeling and Simulation plays a vital role in digital twin realization.

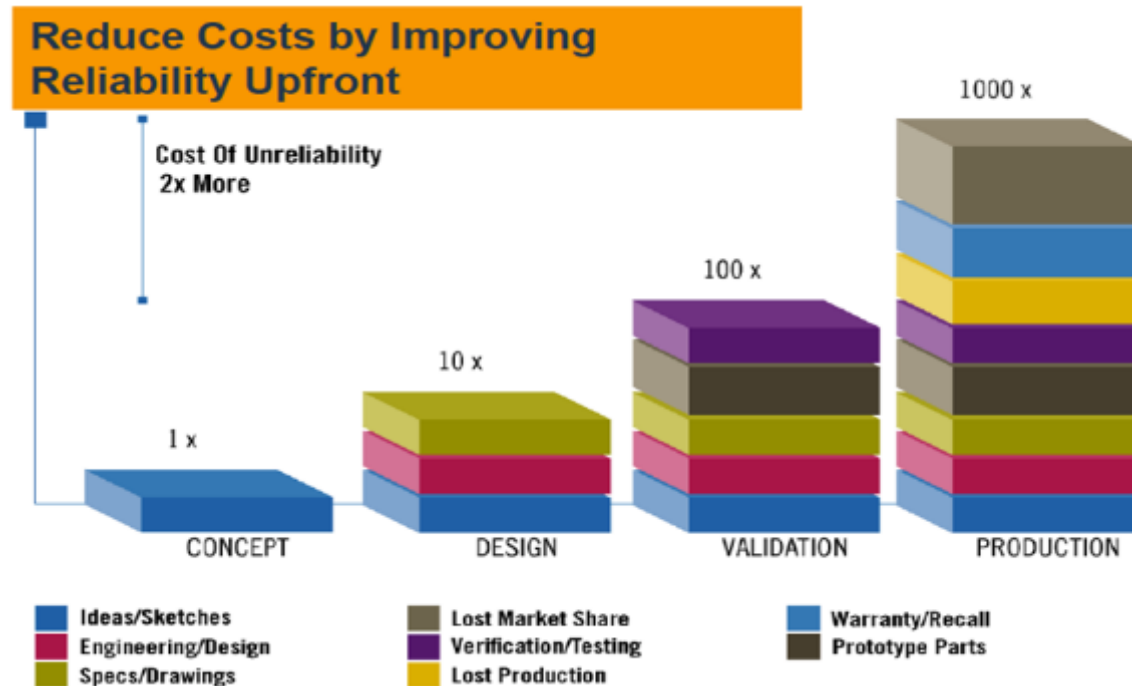
2020 Edition

- Minor revisions on current sections
- Sections on
 - Materials Characterisation Techniques
 - System level modelling
- Alignment with other chapters
- Review metrics



Importance of Forums like TIE/SIITME

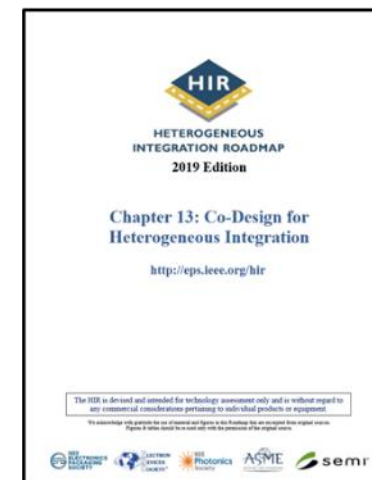
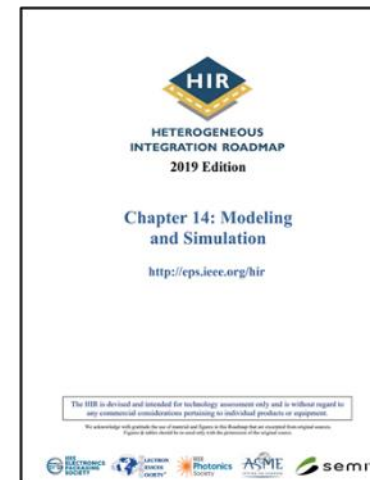
- Economics of Moore's Law Scaling has ended
- Future Scaling through Heterogeneous Integration
- Co-Design and Multi-Physics Modelling Tools Required
 - Die – Package - System



Industry and Designers of Heterogeneous Integrated System

Universities & Research Institutes

Tool Vendors



Industrial Panel: Introduction to HIR Modelling Goals & Application Challenges

- Session Chairs

- Chair: Chris Bailey, University of Greenwich, UK
- Co-Chair: Pop Ovidiu Aurel, Technical University of Cluj Napoca, Romania

- Introduction Session (14:00 – 14:15)

- *14:00 – 14:15: Short Introduction to the goals of HIR Modelling Mission - Chris Bailey, Co-Chair of HIR Modelling and Simulation Chapter.*

- Presentations (14:15 – 15:15)

- *14:15-14:30: Simulation driven design flow of high-speed data links in the automotive industry – Catalin Negrea, Continental Automotive, Romania*
- *14:30 – 15:00: Electromagnetic Simulation for EMC/EMI – Irina Munteanu, Dassault Systemes SIMULIA, TU Darmstadt*
- *15:00 – 15:15: Finite element analysis in electronics – Marius Tarnovetchi, Vitesco.*

- Q&A Session: Moderated online session (15:15 – 15:30)