Challenges of Embedded DDR Memory Interface Integration for the Automotive Industry

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Summary: With the ongoing developments towards autonomous driving and the complex HMI (Human-Machine Interface) requirements, today's electronics engineers are faced with the difficult challenge of designing high bandwidth interfaces under automotive reliability constraints. Double data rate (DDR) interfaces have become widely spread also in the automotive segment due to the ever-increasing image processing bandwidth required for high-resolution and three-dimensional multi-layered graphics. This presentation is focused on the challenges and pitfalls associated with the implementation of memory interfaces in the context of high-volume production and environmental stress that are imposed by automotive standards.

Keywords: EM simulation, signal integrity, DDR memory interfaces

Motivation and Description of Work

The memory requirements for image processing have increased dramatically in last years due to large scale adoption of high resolution displays and 3D graphics. The introduction of LPDDR4 to the automotive market has marked the shift of clock frequencies above 1GHz. Figure 1 present the block diagram for the simplest architecture for a point-to-point system: a single rank, single component memory with 32 data lines (bits). It can be observed that while clock and data strobe lines are differential, the address/command and data lines are still single-ended, meaning that the signal spectrum that must be considered in order to assure signal integrity exceeds 15 GHz. This figures in combination with PCB fabrication tolerances and extended temperature requirements lead to a large parameter set involved in the worst-case scenario definition. A comprehensive assessment on signal quality can only be made by using a simulation-driven design flow based on a selective design of experiments (DoE) approach.

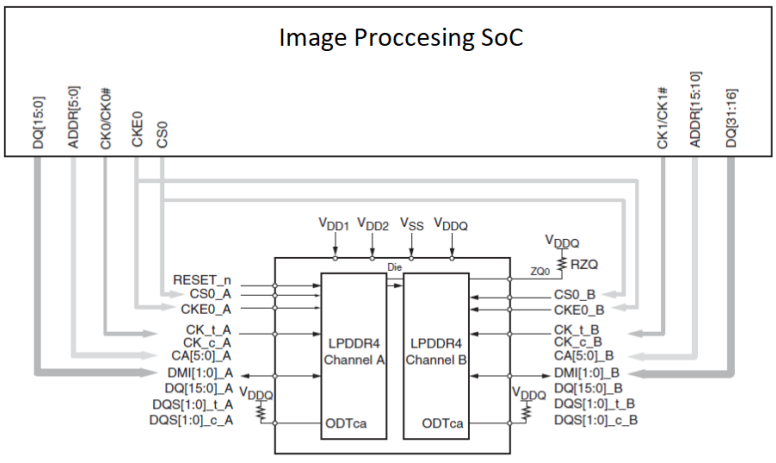

Fig. 1: LPDDR4 x32 interface block diagram

Results

By using interconnect modelling software, the impact of several factors, including prepreg and copper layer thickness, Dk (dielectric constant) variation with frequency and etching factor, on the value of PCB trace impedance can be simultaneously analysed. A set of corner case interconnect models can be extracted and then used in the transient simulation of the data channel. Figure 2 shows the results of transient domain simulation of an LPDDR4 data line during read operation. The data eye variation caused by the impedance changes of the interconnect due to PCB manufacturing tolerances is in the range of 100mV. Given the low margin of DDR4 input thresholds, such variations represent a point of concern especially in combination with IC process corners. Due to the single-ended bus nature of the data lines one other critical topic is crosstalk. This will be further discussed in the presentation.

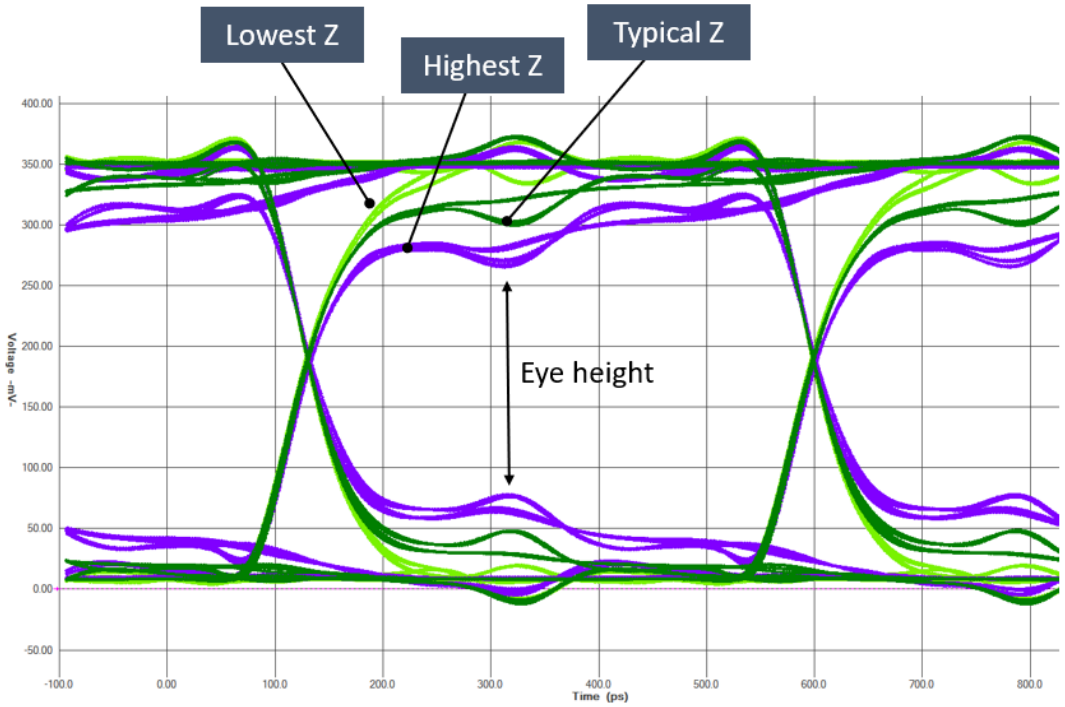

Fig. 2: Effect of PCB fabrication tolerances on the data signal eye diagram of a LPDDR4 interface

This presentation will briefly cover the basic simulation steps required for designing a DDR memory interface with the primary goal of assuring signal integrity, while emphasizing the need of a detailed analysis for the impact of factors such as PCB material parameter variation, PCB fabrication tolerances and IC process corners. Pitfalls of a conventional design approach will be identified and discussed in the context of automotive requirements.