

Solder Joint Interconnections in Automotive Electronics: Design-for-Reliability and Accelerated Testing

E. Suhir,

Departments of Mechanical and Materials and Electrical and Computer Engineering,
Portland State University, Portland, OR, USA; Department of Electronic Materials, Technical
University, Vienna, Austria, and ERS Co., Los Altos, CA, USA, suhire@aol.com

Summary

This presentation is based on the author's recent work on design-for-reliability and accelerated testing of solder joint interconnections (SJIs) employed in electronic packaging. The emphasis is on automotive applications. The following three critical and challenging problems are addressed:

- 1) Could inelastic strains in the solder material, particularly the one of the second level of interconnections, be avoided by a rational design, and, if not, could the sizes of the inelastic strain areas be predicted and minimized?
- 2) Considering that the difference between an highly reliable and an insufficiently reliable electronic product is "merely" in the level of its never-zero probability of failure, and that the SJI is typically the most vulnerable structural element in an IC package design, could this probability be assessed at the design stage and, if necessary, minimized?
- 3) Should temperature cycling accelerated testing for SJIs be replaced by a more physically meaningful, less costly, less time- and labor- consuming approach, especially having in mind automotive applications?

Keywords: Solder joint interconnections; physical design-for-reliability; probabilistic assessments; avoiding inelastic strains; accelerated testing techniques.

Motivation and Description of Work

1) SJIs are the most vulnerable structural elements in the today's IC packages. That is mostly because the solder material (typically in the peripheral portions of the assembly, where the interfacial thermal stresses are the highest) experiences inelastic strains, and, hence, is subjected to low cycle fatigue conditions. As the consequence of that the fatigue lifetime of the material is often much shorter than required for a particular application. There is an obvious incentive therefore to consider and explore ways to bring down the induced stresses and strains in the solder material, even, if possible, to an extent that the inelastic strains in it are avoided. Then the material will perform within the elastic range, and its fatigue lifetime will be much longer. Accordingly, several novel and promising approaches to the design-for-reliability of SJIs have been suggested and the corresponding predictive models, based on analytical ("mathematical") modeling and confirmed by finite-element-analysis (FEA), were developed. The models enable to evaluate the expected reduction in the stress level and in the bow (warp) of the assembly and to see, based on the computed data, what could possibly be done to reduce stresses and deformations of the SJIs of either level of interconnections.

2) The era in the materials science, when "we heat, we beat and we pray" has gone. In the today's materials science world, when the behavior and performance of a material, and the operational reliability of an electronic product is critical, ability to predict (quantify) this performance (reliability) and, if possible and advisable, even specify it, is imperative, and since nothing is absolutely certain, such a prediction should be preferably done on the probabilistic basis. Accordingly, the probabilistic design-for-reliability (PDR) concept is suggested and applied with an intent to predict, based on the highly focused and highly cost-effective failure-oriented-accelerated testing (FOAT) conducted for a SJI system, whether

flip-chip type or BGA or CGA type, the probability of possible failure in the field. As a rule, the recently suggested Boltzmann-Arrhenius-Zhurkov (BAZ) model was applied to predict this probability from the FOAT data.

3) Temperature cycling as the most widespread today accelerated test is costly, time- and labor consuming, but, most importantly, can result in misleading information, since testing is done in a wide temperature range, much wider than what the material might encounter in actual operation, and, as is known, material's properties are temperature dependent. Because of that, there is a clear motivation to find another test vehicle that would be less costly and more physically meaningful. Since the highest stresses occur in SJIs at low temperature conditions and crack propagation is accelerated by random vibrations, a low-temperature/random-vibrations bias is considered as an attractive substitute for temperature cycling.

Results

1) Effective technologies for a rational design of low stress SJIs, even sometimes below the yield stress, are suggested and confirmed by analytical modeling and illustrated by numerical data. The two major means are a) using SJIs with elevated stand-off height of the joints and/or b) employing inhomogeneous SJI systems, in which solders with lower moduli and, if possible and feasible, also with lower soldering temperatures are used [1]

2) Flexible and physically meaningful BAZ model is suggested and implemented in application to SJIs, and particular to those used in automotive engineering, when high or low temperatures are possible, and elevated vibration loading is typical, as well as elevated humidity [2]

3) Combination of low-temperature, random-vibrations and elevated humidity stressors are suggested as an attractive substitute for temperature cycling. The random vibrations are considered as a white noise of the given ratio of the acceleration amplitudes squared to the vibration frequency. Testing was carried out for two PCBs, with surface-mounted packages on them, at the same level (with the mean value of 50g) of three-dimensional random vibrations. In addition, one board was subjected to the low temperature of $-20^{\circ}C$ and another one – to $-100^{\circ}C$. It has been found, by preliminary calculations, that the solder joints at $-20^{\circ}C$ will still perform within the elastic range, while the solder joints at $-100^{\circ}C$ will experience static inelastic strains. No failures were detected in the joints of the board tested at $-20^{\circ}C$, while the joints of the board tested at $-100^{\circ}C$ failed after several hours of testing [3].

References

- [1] E. Suhir, "Analytical Thermal Stress Modeling in Electronic and Photonic Systems", ASME App. Mech. Reviews, vol.62, No.4, 2009.
- [2] E. Suhir, "Probabilistic Design for Reliability", Chip Scale Reviews, vol.14, No.6, 2010
- [3] E. Suhir and R. Ghaffarian, "Solder Material Experiencing Low Temperature Inelastic Thermal Stress and Random Vibration Loading: Predicted Remaining Useful Lifetime", Journal of Materials Science: Materials in Electronics, vol.28, No.4, 2017