

EMC-Aware System Design - A focus on Integrated Circuits



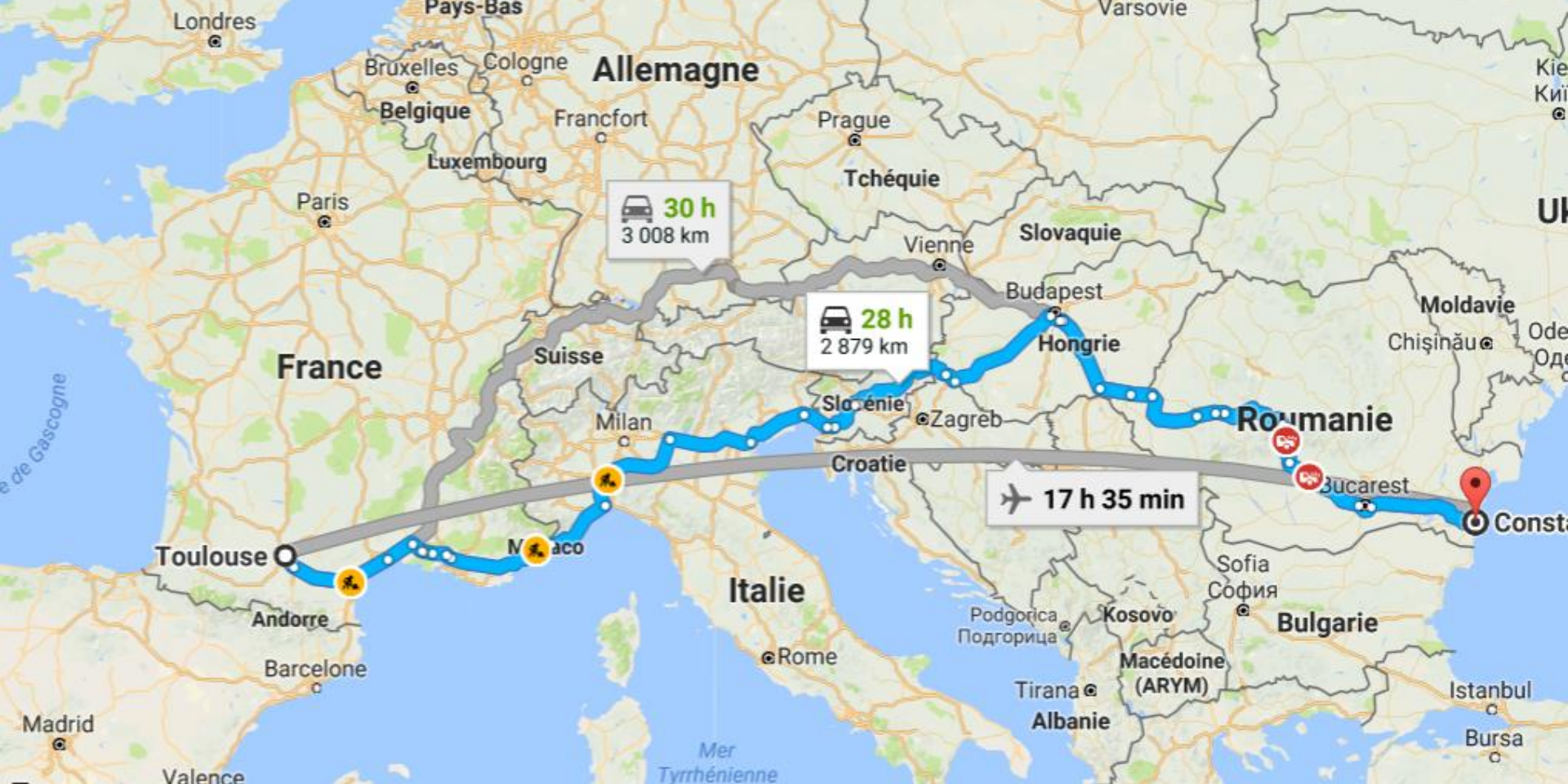
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Professor

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www.ic-emc.org

INSA TOULOUSE - FRANCE



A350XWB
Shaping efficiency



Airplanes



Rugby

Toulouse - the best place to be a student in France



Studying



Université
de Toulouse

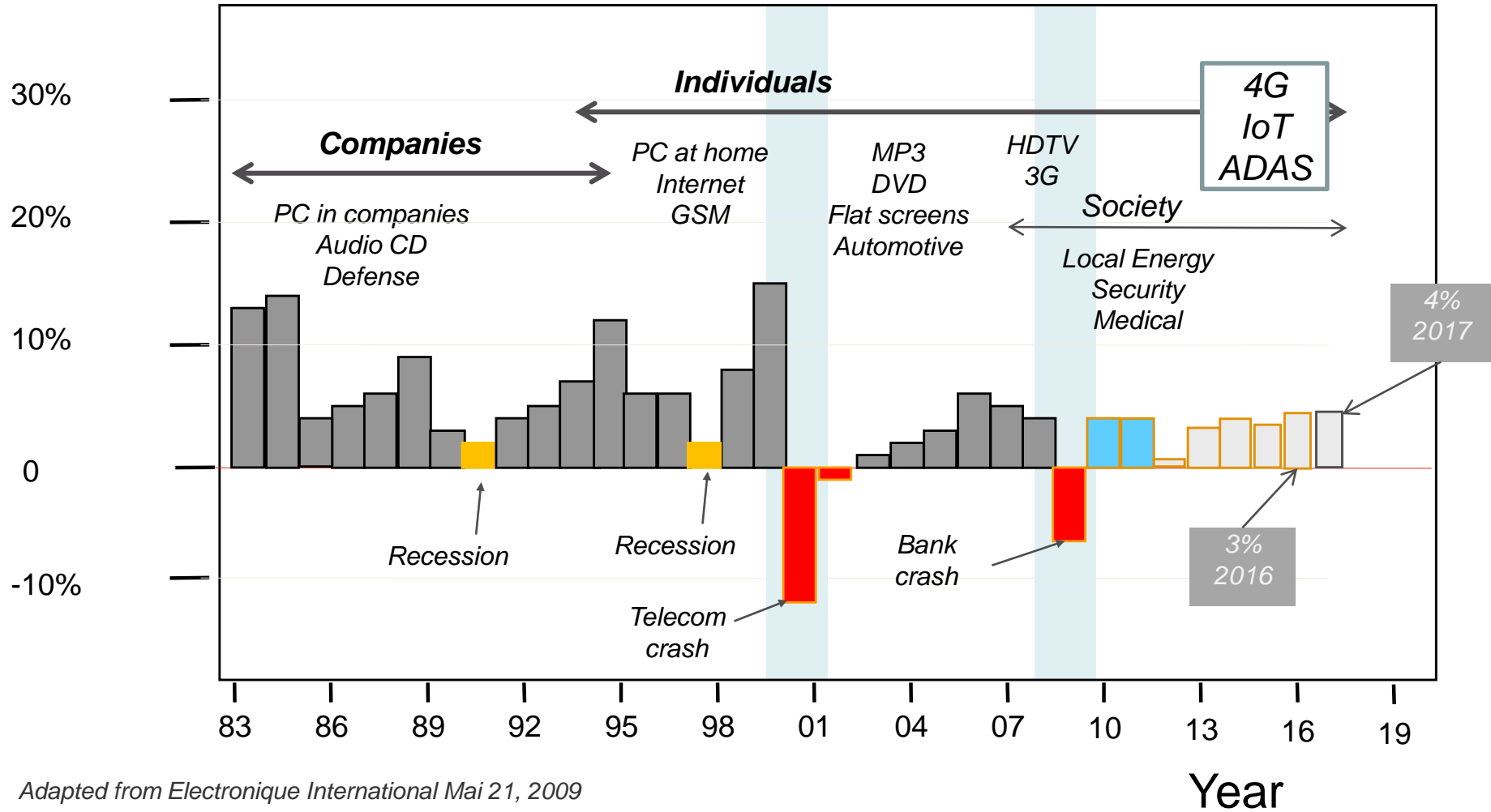
- **General context**
- **Integrated Circuits**
- **Electromagnetic
Compatibility**
- **Design Guidelines**



1 GENERAL TRENDS

THE ELECTRONIC MARKET GROWTH

Market Growth

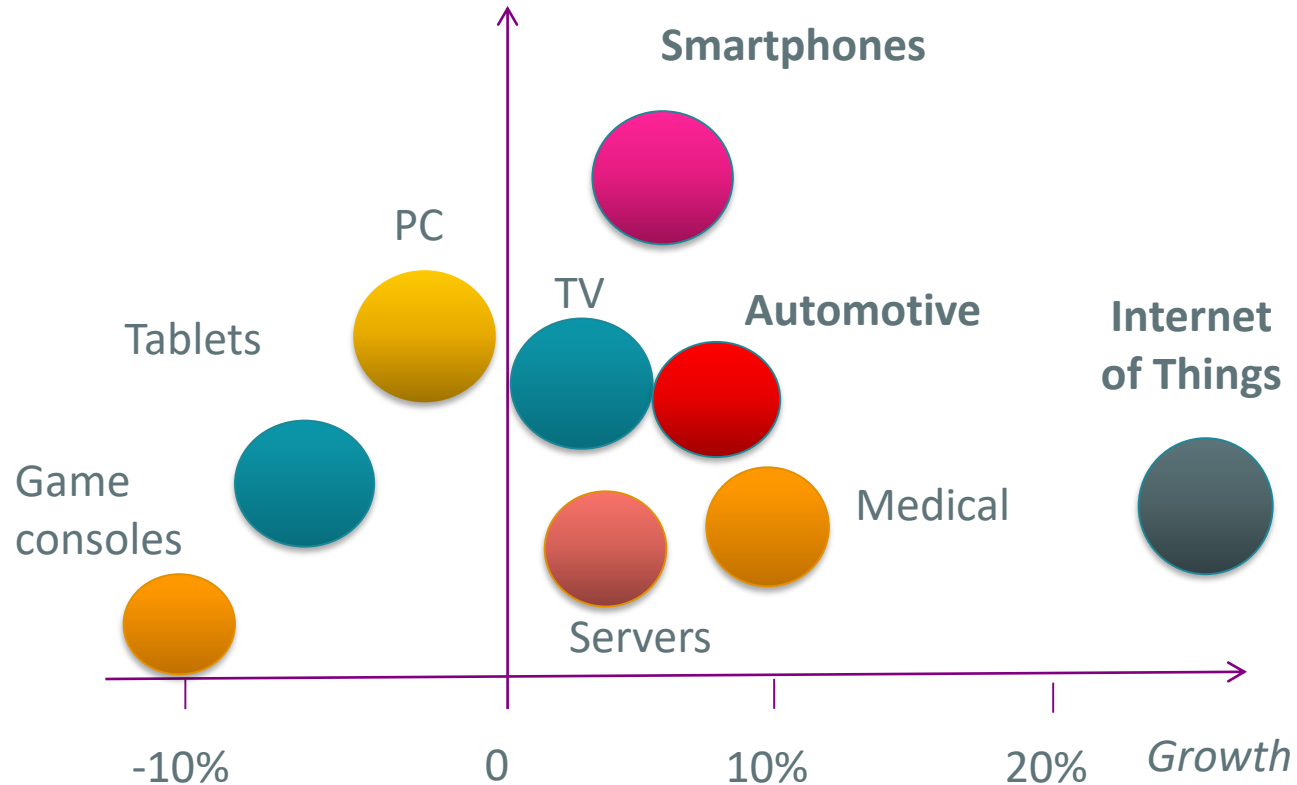


Adapted from *Electronique International* Mai 21, 2009

VISION 2020

- Increasing disposable income,
- Expanding urban population,
- Growing internet penetration and
- Availability of strong distribution network

*Share of system sales
2020 vs 2015*



<https://www.gsmainelligence.com/>

GLOBAL DATA

Mobile connections, including M2M
Oct 2017

8,372,794,953

▲ 4.70%

Unique mobile subscribers
Oct 2017

5,082,304,193

▲ 4.76%

Revenue/year
FY 2015

\$1.06T

▲ 2.18%

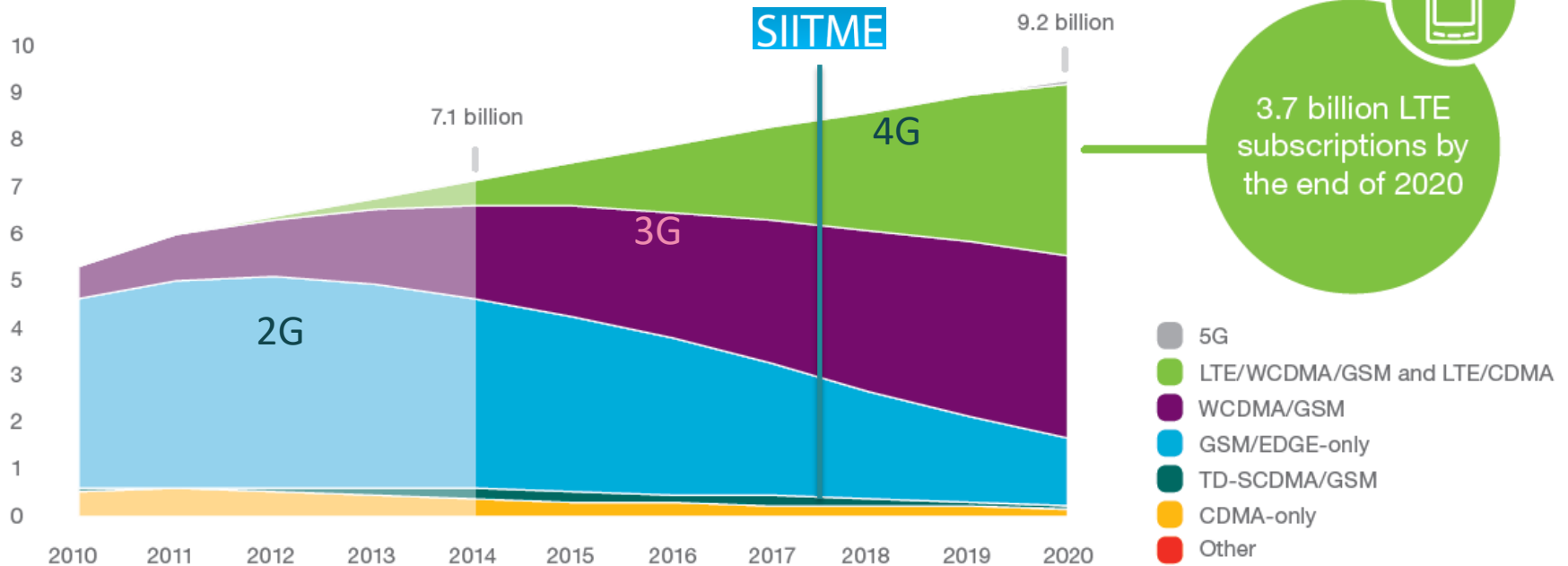
ARPU/month
FY 2015

\$10.25

▼ -2.78%

Source: GSMA Intelligence 2017, current year-end data except interpolated subscribers and connections

Mobile subscriptions by technology (billion)



<http://www.ericsson.com/ericsson-mobility-report>

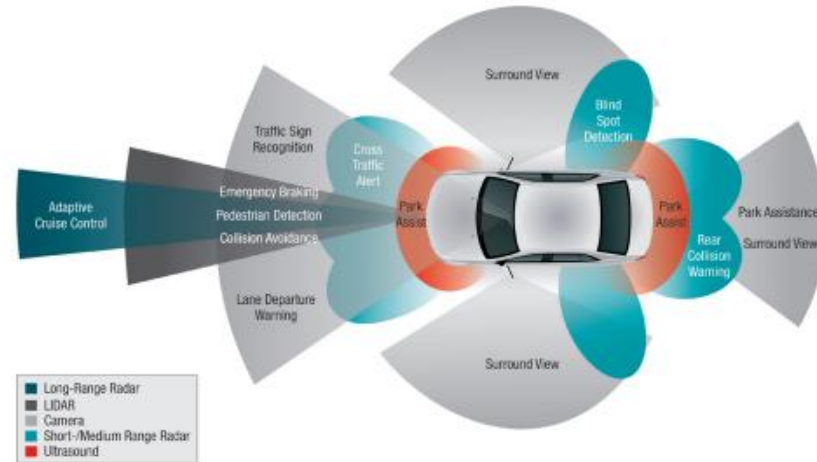


- Growth in 2016 was **stalling** (+5% smartphones)
- Consumer demand was **sluggish** (tablets, laptops).
- Demand for **Internet of Things** (IoT) wasn't growing fast enough to offset declines
- **Price, security and ease-of-use** remain barriers to the adoption of new IoT devices and services.

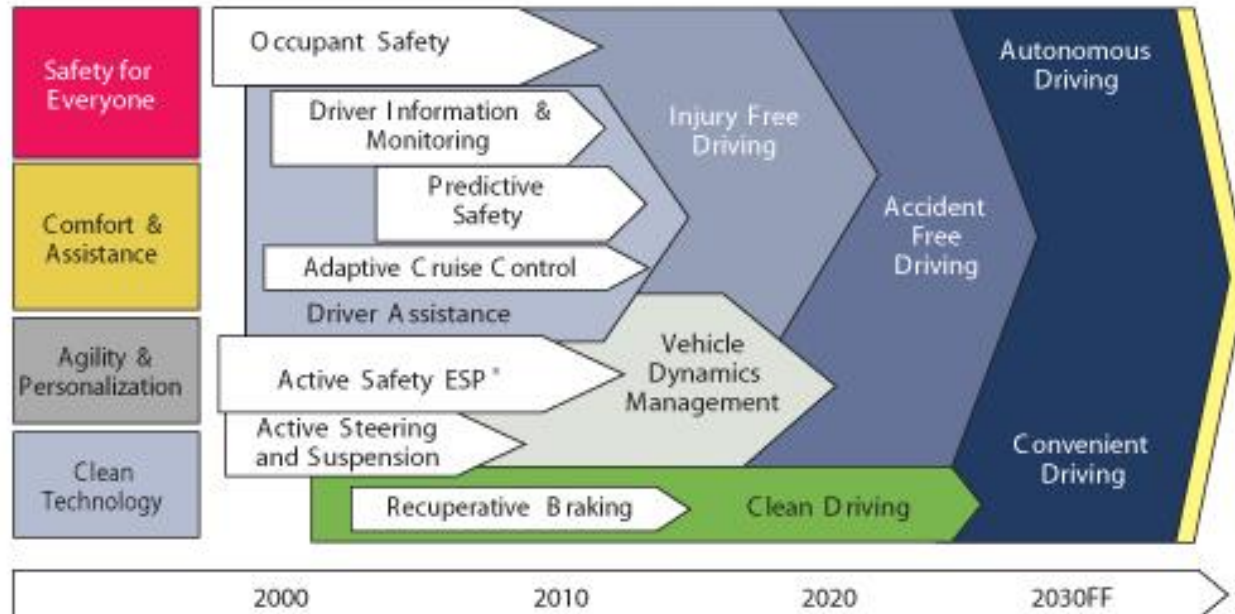


TOWARDS AUTOMATIC DRIVE

- 2020 : **Injury-free** driving
- 2030: **Accident-free** driving ?
- 2040: **Autonomous** driving?



VISIONS FOR VEHICLE MOTION AND SAFETY

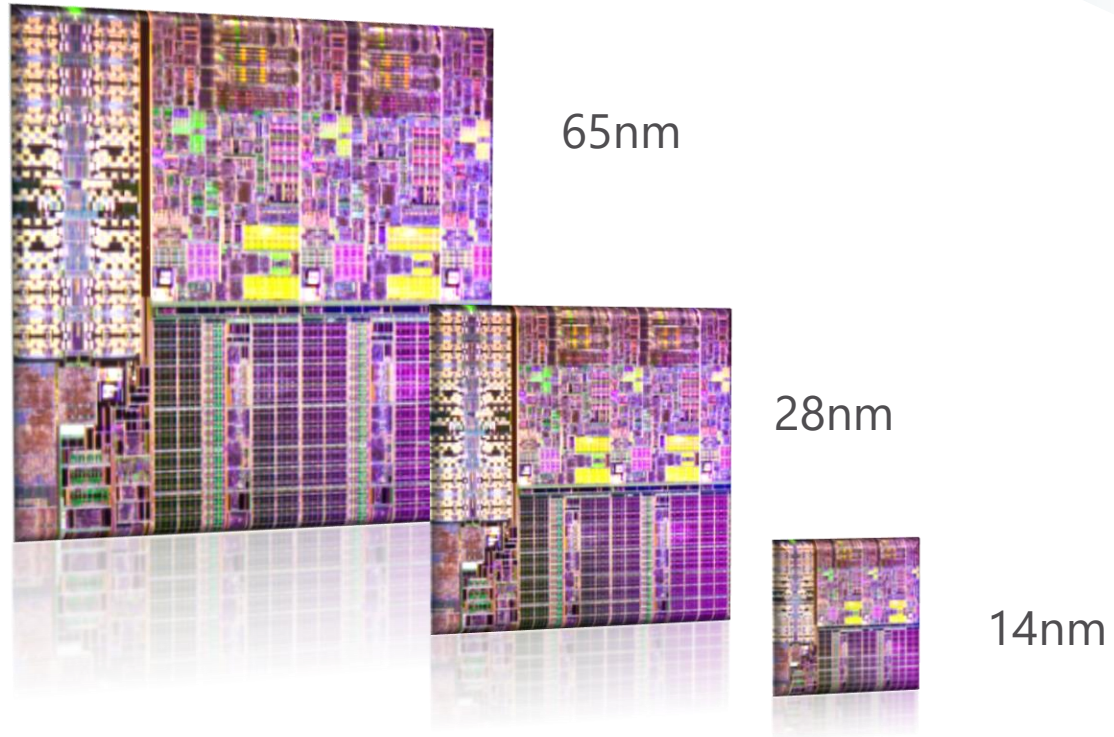




2 TECHNOLOGY TRENDS

SCALE DOWN BENEFITS

- **Smaller**
- **Faster**
- **Less power consumption**
- **Cheaper (if you fabricate millions)**
- **Room for other devices**

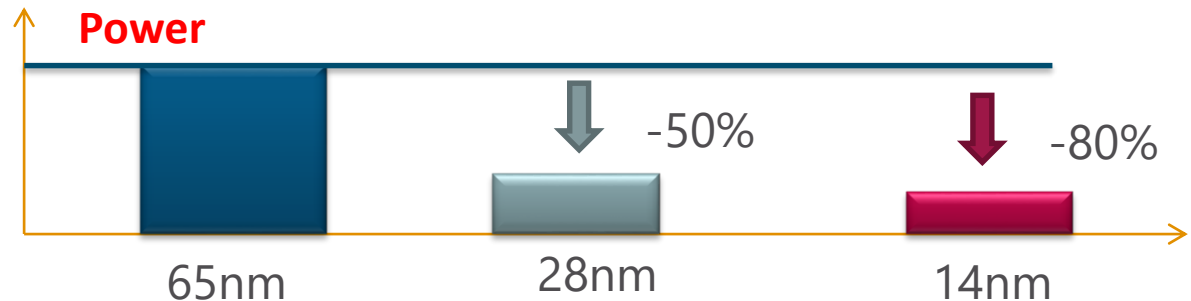


Processors

Memory

Security

Sensors



MOBILE COMMUNICATIONS

SIITME

Technology

130nm

90nm

45nm

28nm

14nm

5nm

Complexity



100M

250M

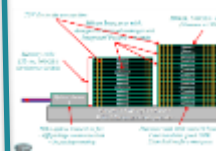
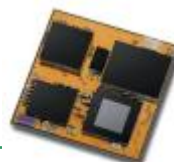
500M

2G

7G

150 G

Packaging



Mobile generation

3G

3G+

4G

4G+

5G

2004

2007

2010

2013

2016

2020

Embedded blocks

Core+
DSP
1 Mb
Mem

Core DSPs
10 Mb
Mem

Dual core
Dual DSP
RF
Graphic Process.
100 Mb Mem
Sensors

Quad Core
Quad DSP
3D Image Proc
Crypto processor
Reconf FPGA,
Multi RF
1 Gb Memories
Multi-sensors

?

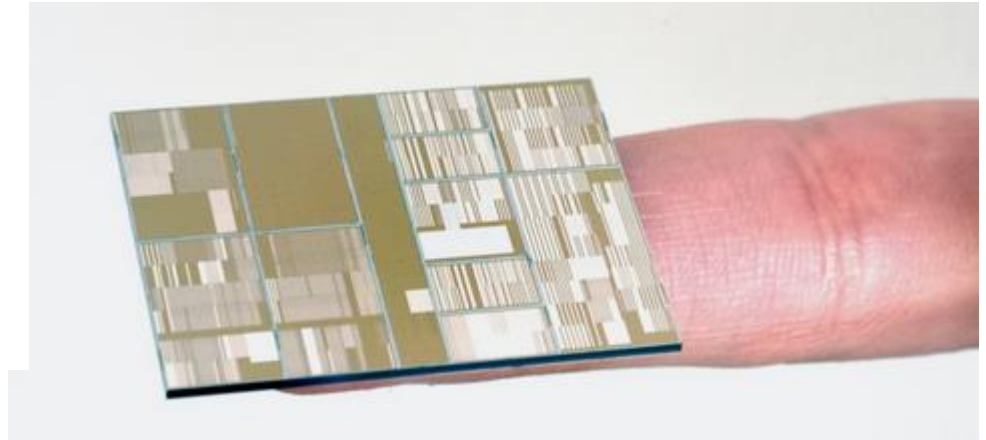


GOING ATOMIC SCALE

- 14-nm Xeon by Intel™



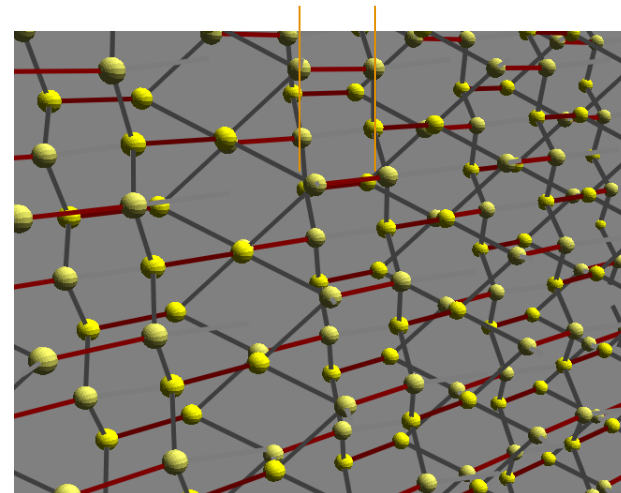
- IBM, GlobalFoundries, Samsung, SUNY first 7-nm testchip 2017



- Qualcomm™ Snapdragon X50

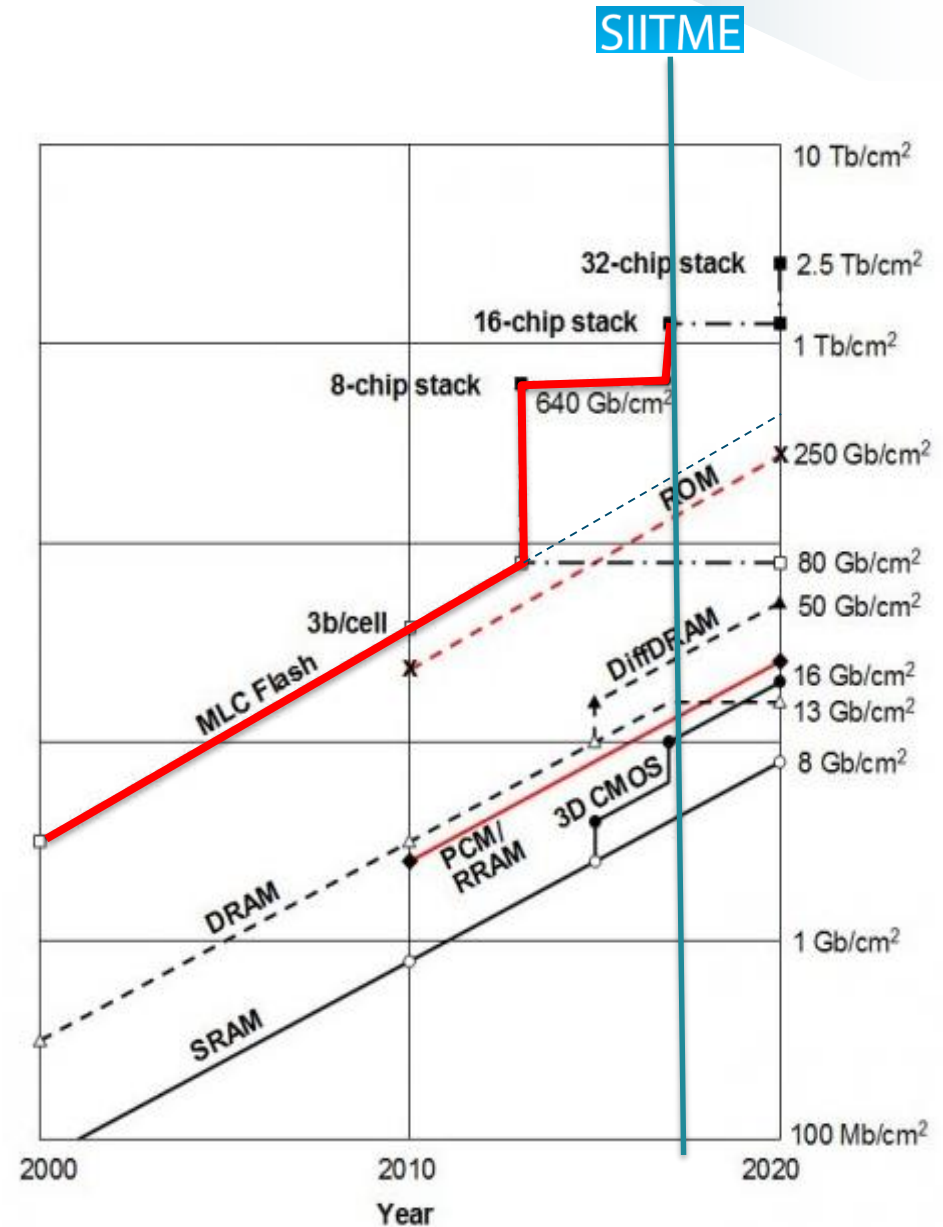
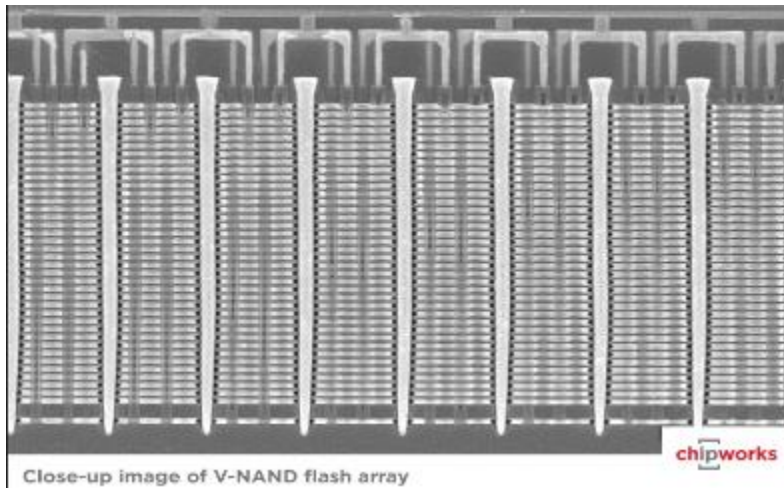


Si lattice: 0.23 nm

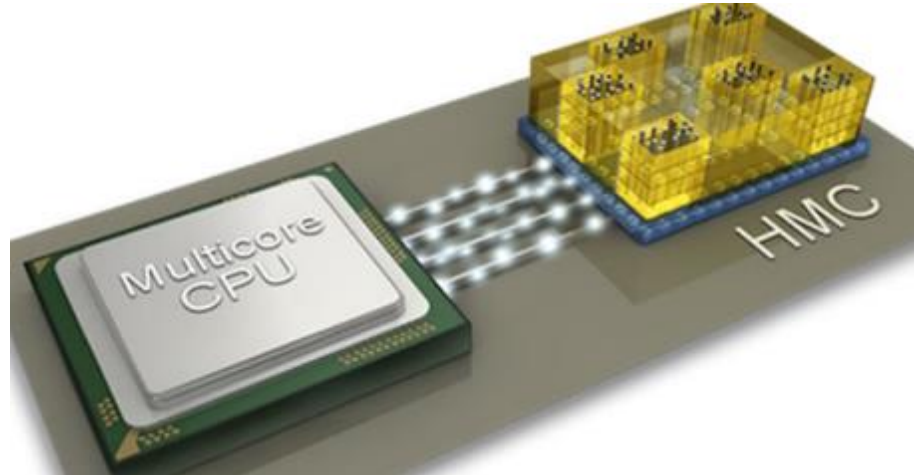
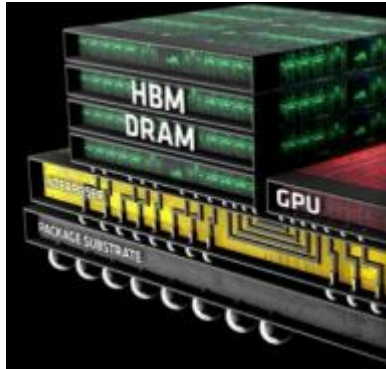


Stacked process layers

- 8, 16, 32 layers of active devices
- 1 tera-bit/cm² achieved 5 years ahead from roadmaps



3D IC TECHNOLOGY

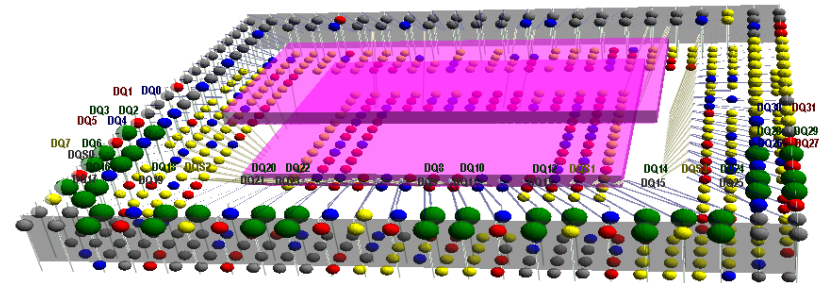
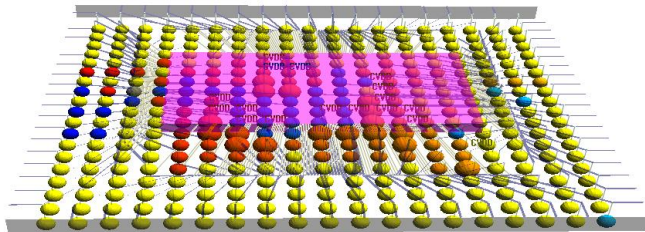
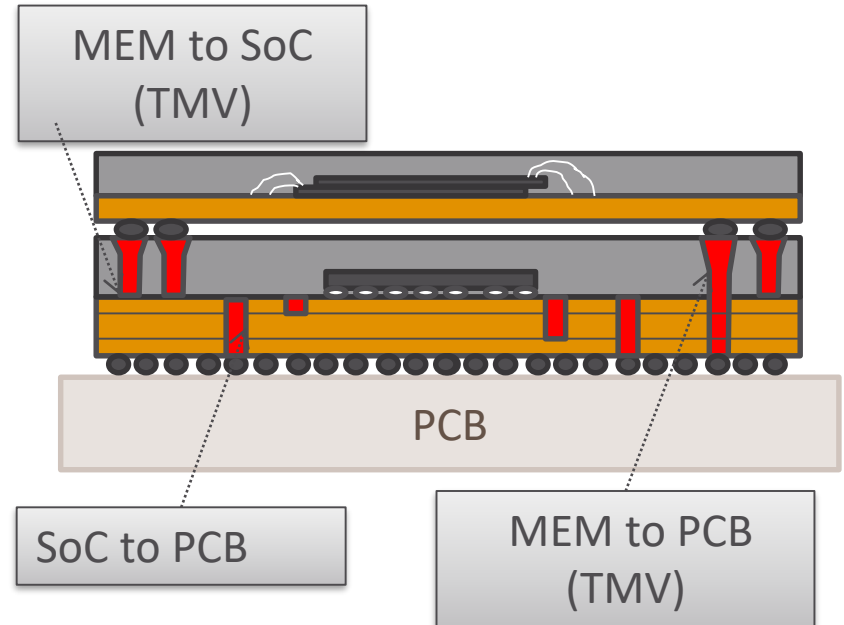
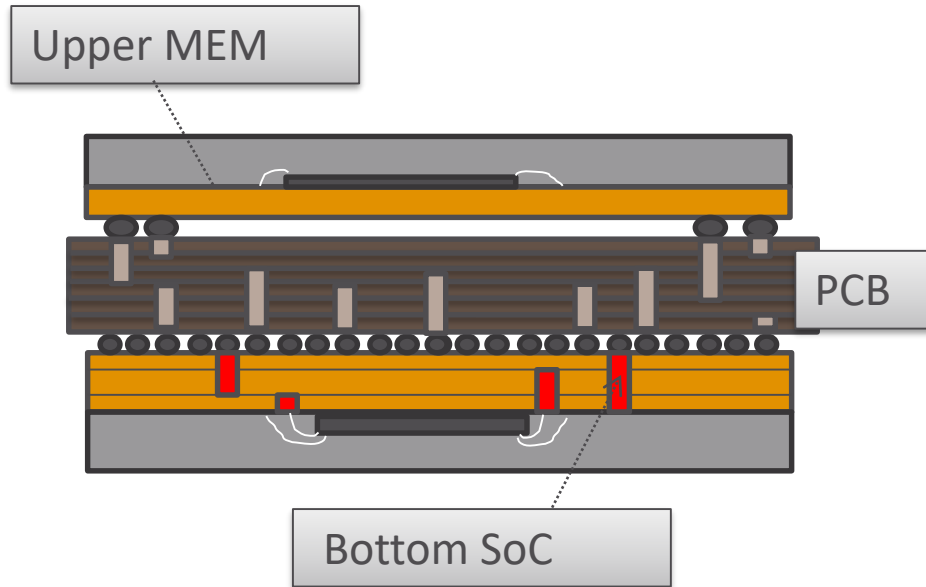


High Bandwidth
Memory (HBM)
Hybrid Memory
Cube (HMC)

	HBM2	HMC Gen3
Density	8 GB (4GB)	8 GB (4GB)
Bandwidth	256 GB/s	480 GB/s (320 GB/s)
IO	Parallel (1G – 2G), 8 channels, 128b per channel	SerDes (up to 30G), 4(2) links per HMC, 16 lanes/link
Package Type	Si-interposer	Discrete (SerDes)
Expansion Capability	No	Yes, via chaining
Memory Access	DDR	Packet based
Power	Lower	Higher
Memory Suppliers	SK Hynix and Samsung	Only Micron
Thermal Dissipation Req.	High (Logic + DRAM in single 2.5D ASIC package)	Lower (discrete ICs)
Ideal target markets	Graphics, Networking, Less frequently accessed memory, Small form-factor	High-performance Computing, Networking

<http://www.eejournal.com/article/20170102-hbm-hmc/>

GOING 3D – Package on Package

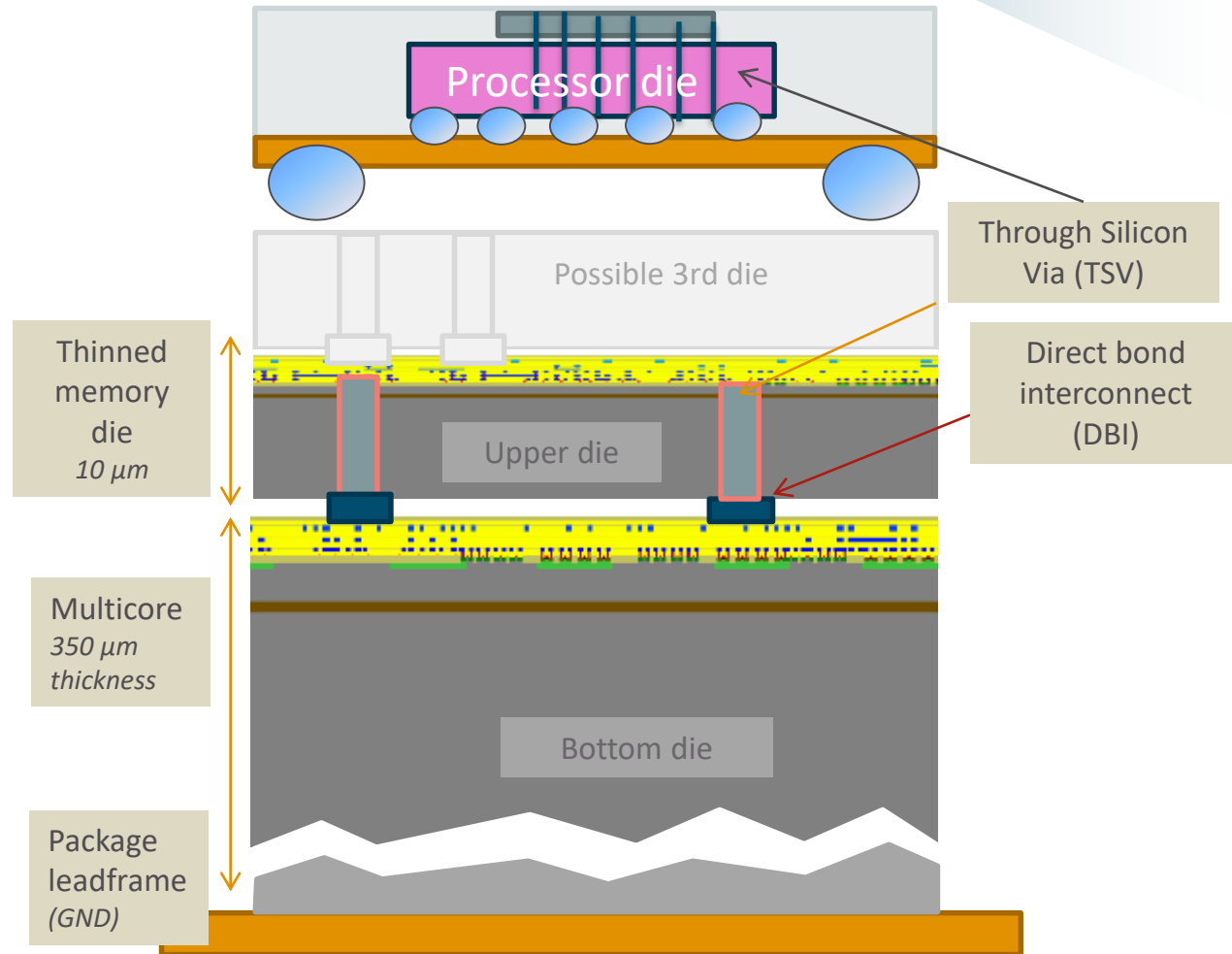


E. Sicard, EMC performance analysis of a
Processor/Memory System using PCB and Package-
On-Package, EMC Compo 2015 Edinburgh

GOING 3D – Stacked Dies

THERE IS PLENTY OF SPACE ON THE TOP

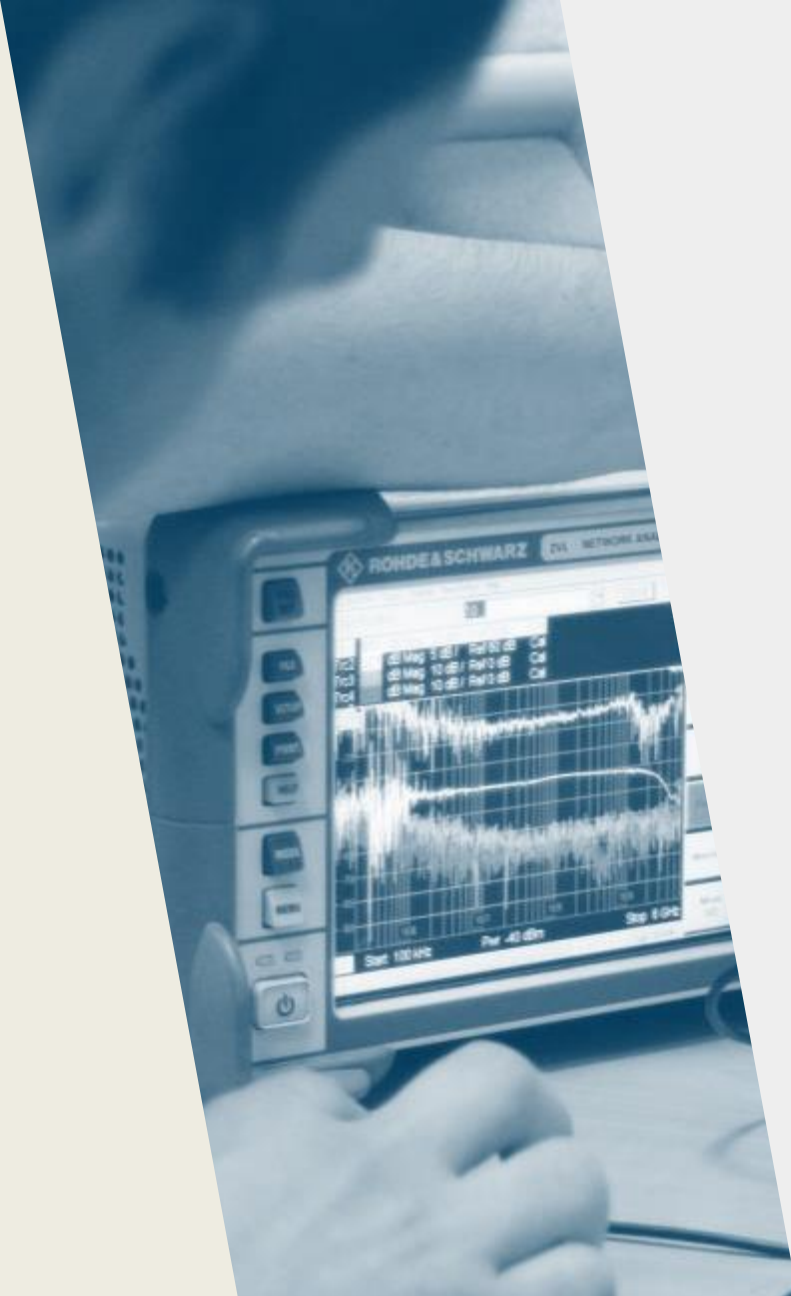
- 3D technology uses stacked dies, through-silicon-vias
- Enables 10-20 Gb/s/pin at 1.0V
- Samsung 3D (Galaxy 6) vs PoP (Galaxy 5) :
 - 30% faster
 - 20% less power
 - Less heat



<http://www.youtube.com/watch?v=Rw9fpsigCfk>

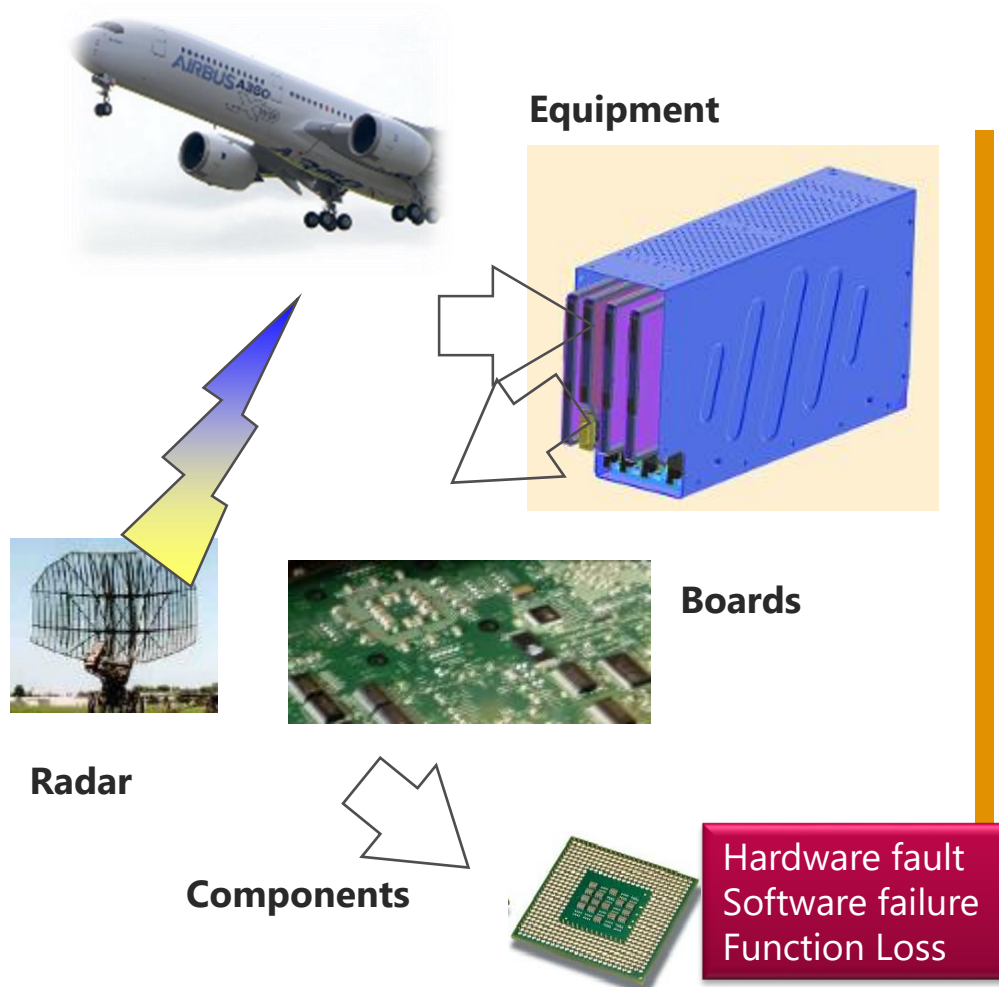
3

ELECTROMAGNETIC COMPATIBILITY



ONE ACRONYM – TWO PROBLEMS

- SUSCEPTIBILITY TO INTERFERENCE**



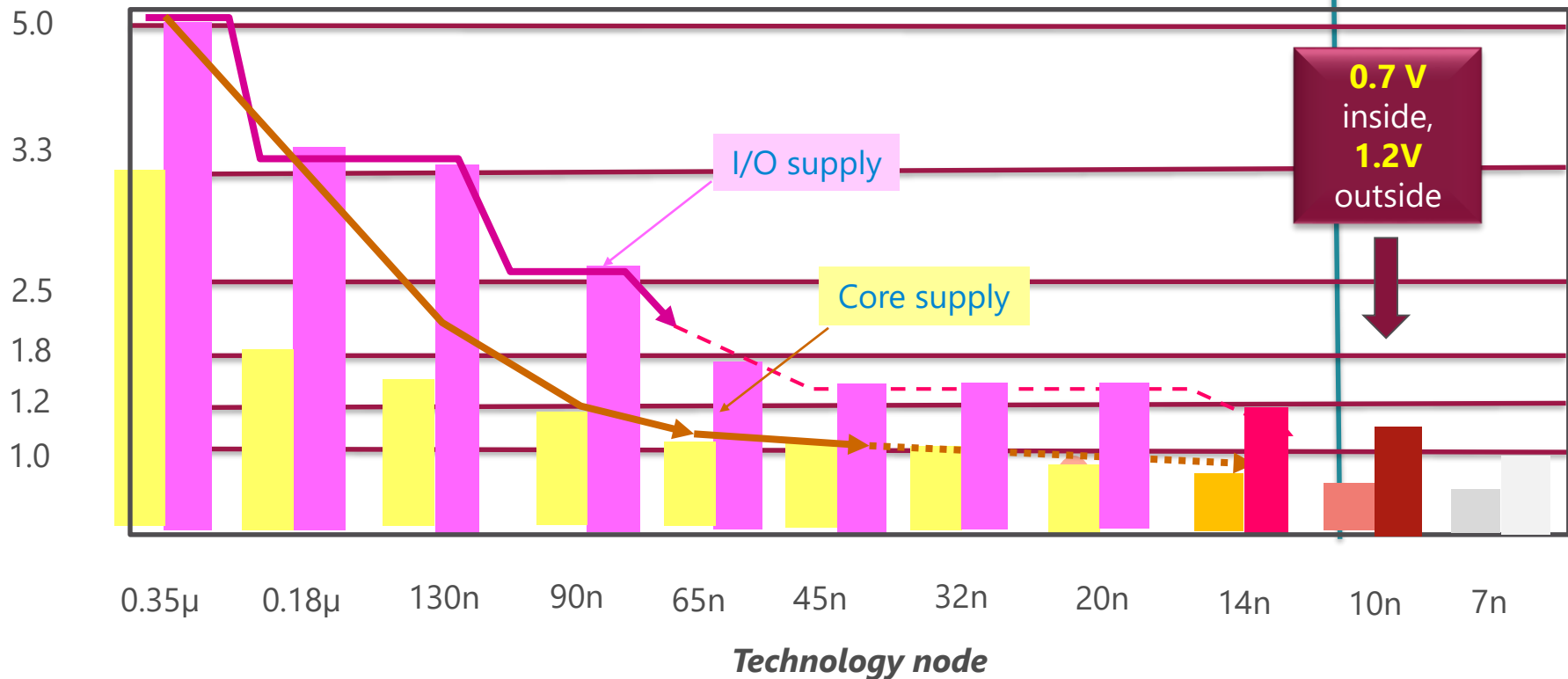
- EMISSION OF PARASITIC NOISE**



SUPPLY VOLTAGE SCALE DOWN

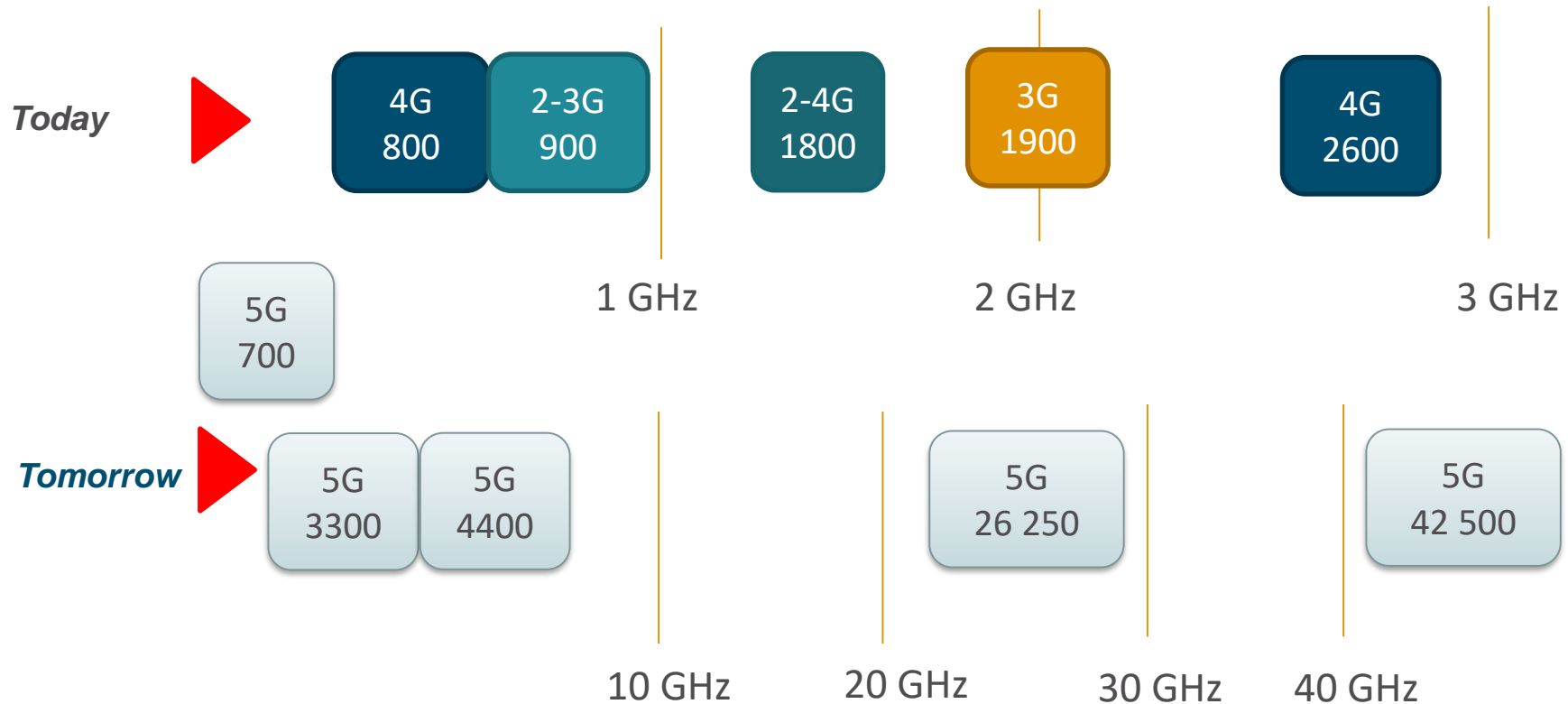
- Less noise margin (<100 mV in 7-nm)

Supply (V)



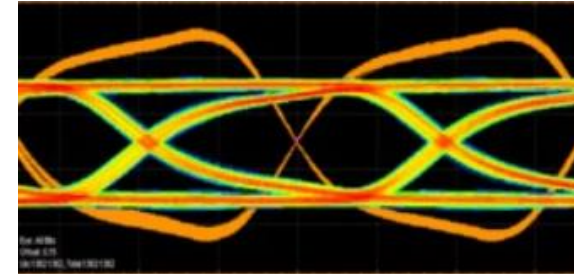


2,3,4,5G mobile frequencies



I/O Technology

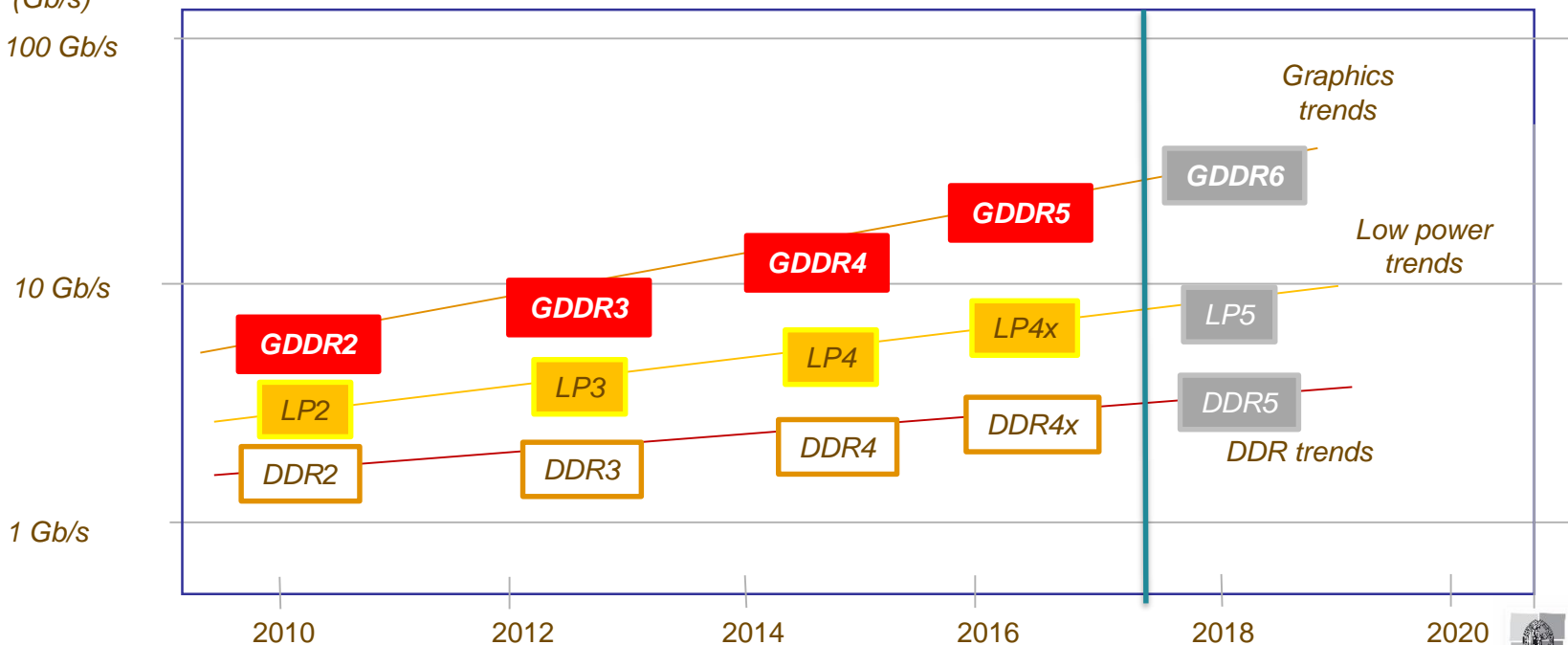
- Multi-Giga-Bit link between processors & memories : video, object recogn., 3D capture
- Generation 4x and 5 on the market
- Generation 6 under development



DDR4x: 230 ps, 0.25 V swing

Data Rate
per pin
(Gb/s)
100 Gb/s
10 Gb/s
1 Gb/s

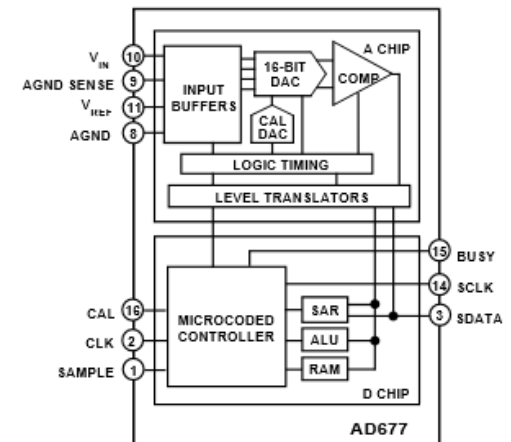
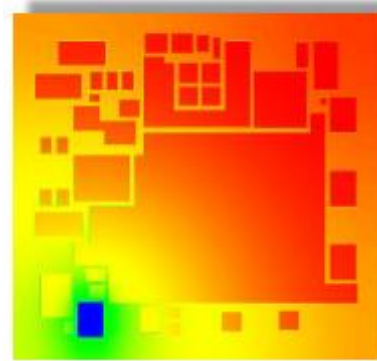
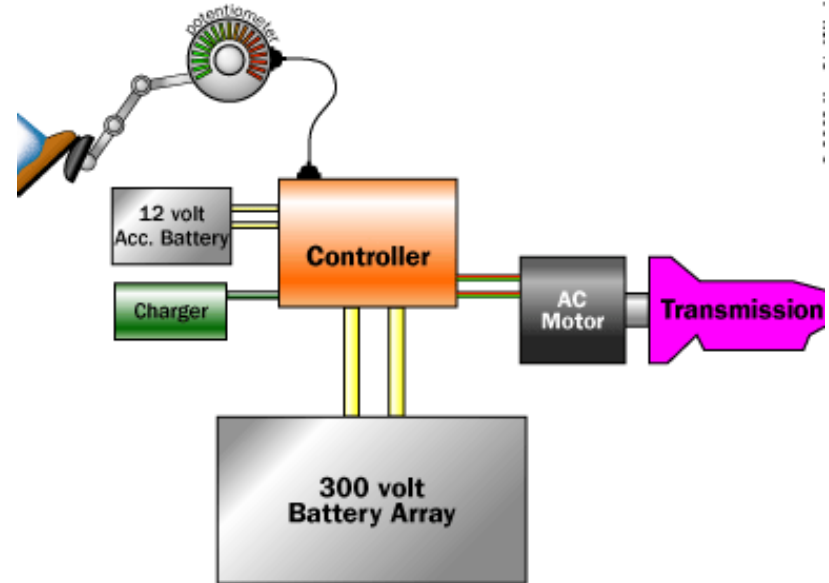
SIITME



WIDE RANGE OF OPERATING VOLTAGES

Technology

- Nano-CMOS operates below 1V, noise margin around 50 mV
- Close to medium voltage (12, 24, 48 V) and high voltage (98, 240, 300, 400, 850 V) functions
- ADC with 16-24 bit resolution work at 10-100 μ V resolution

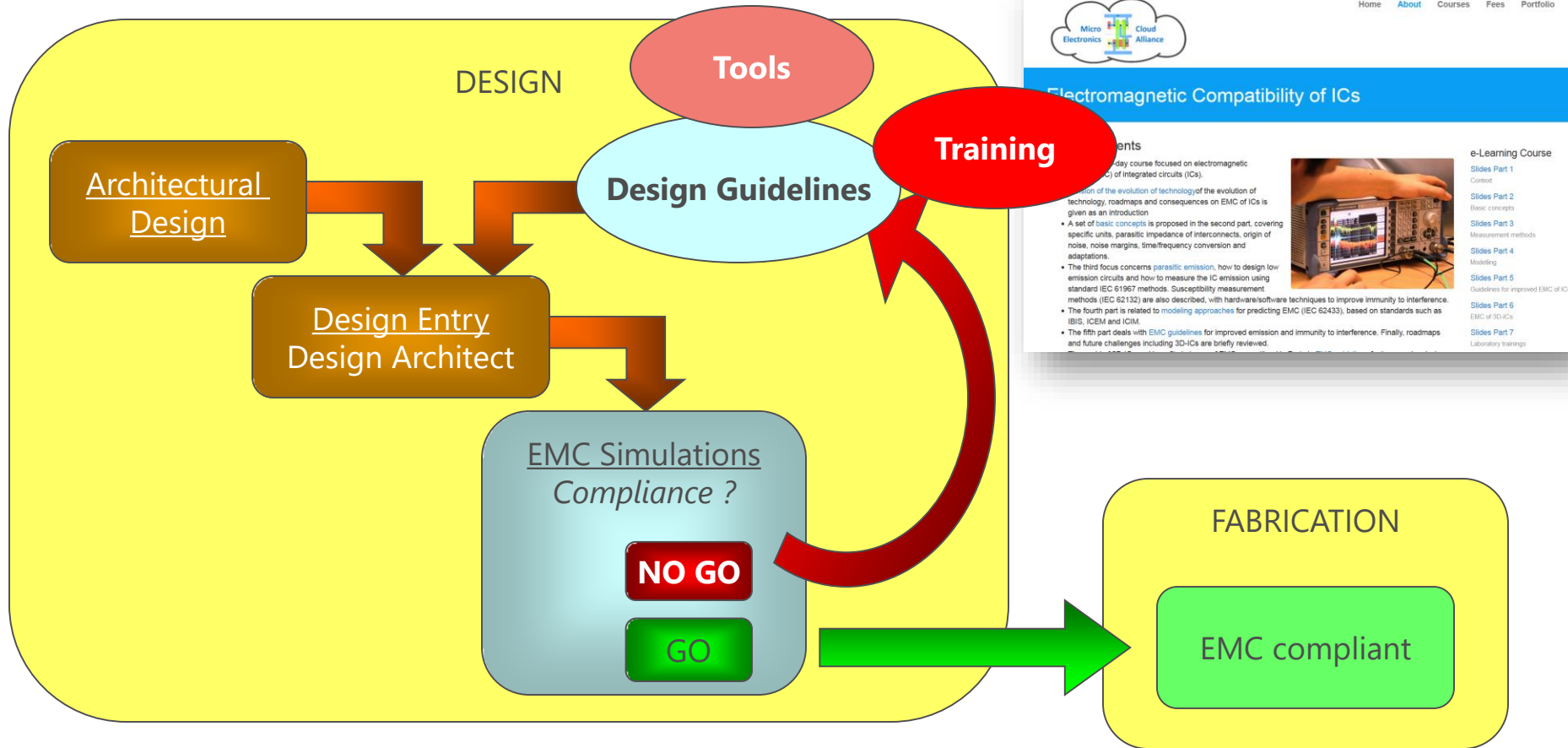




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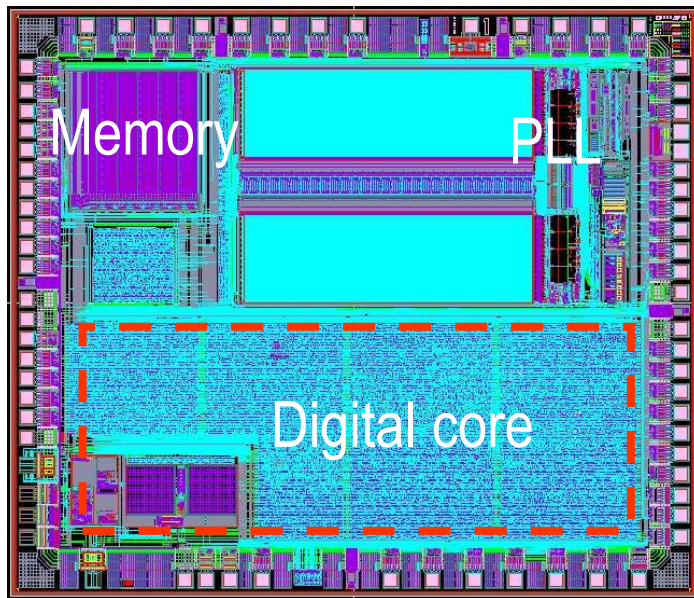
DESIGN GUIDELINES

- Use tools, guidelines and trainings in EMC of Integrated circuits, for improved EMC before fabrication

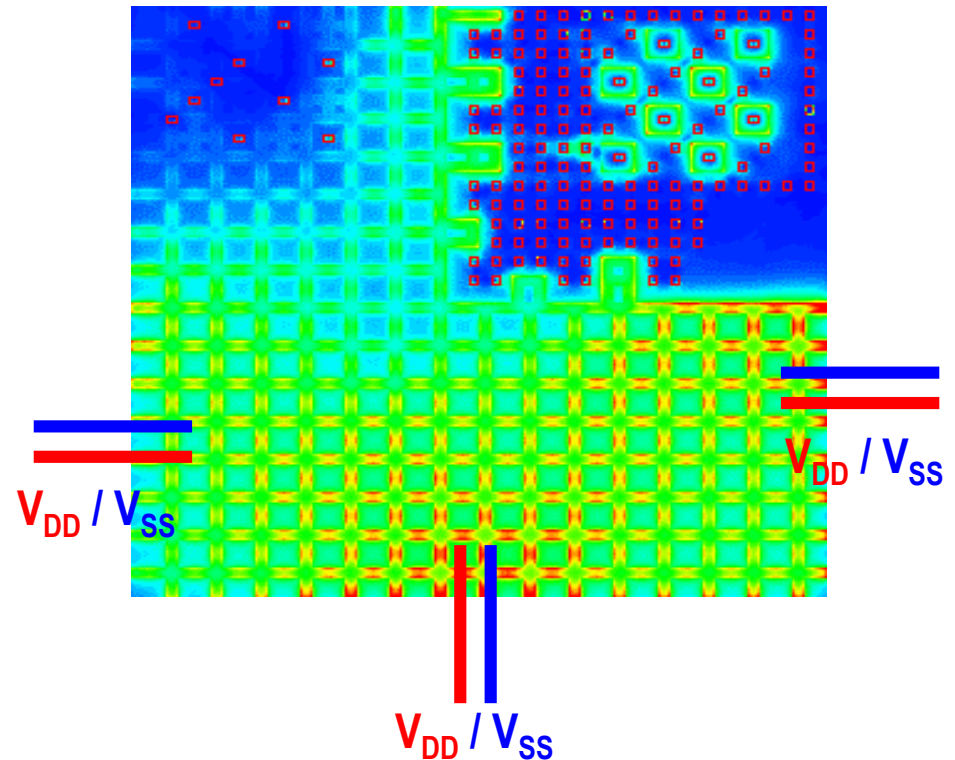


- Place supply pairs close to noisy blocks

Layout view

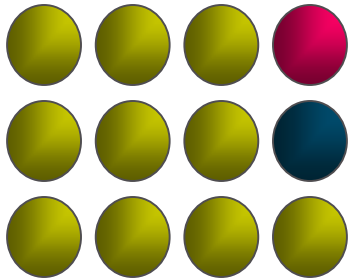


Current density simulation



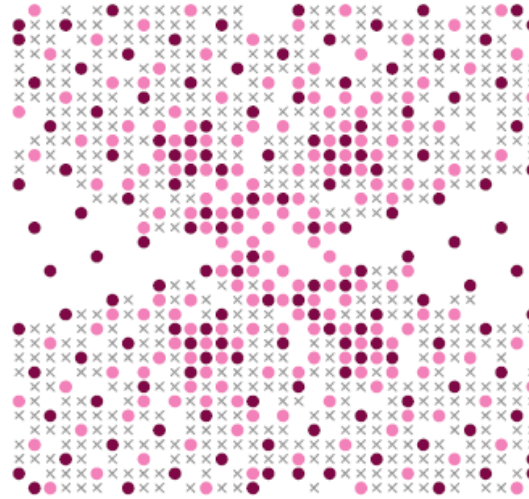
DESIGN GUIDELINES - IOS

- Place enough supply pairs:
Use One pair (VDD/VSS)
for 10 IOs



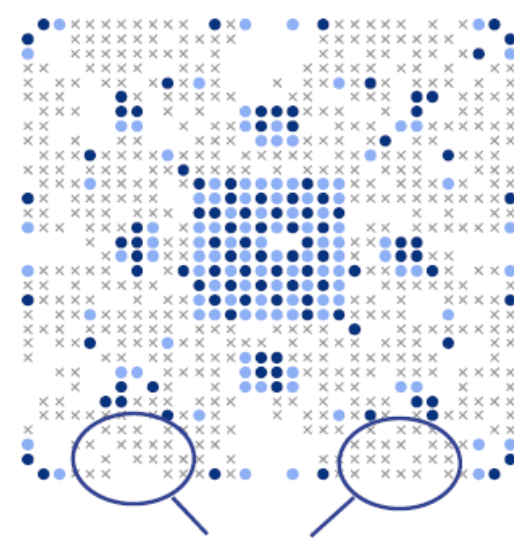
9 I/O ports

Xilinx Virtex-4 FF148

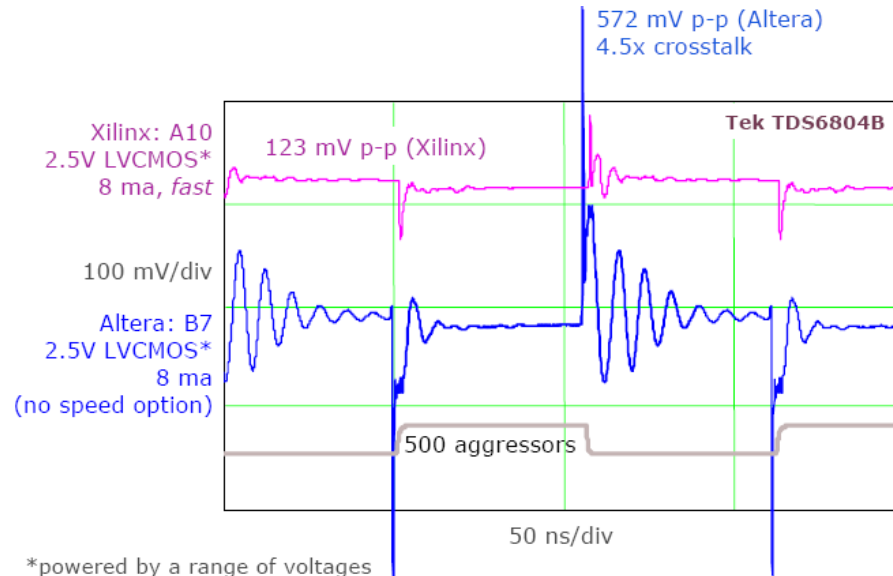


Returns spread evenly

Altera Stratix II F1120

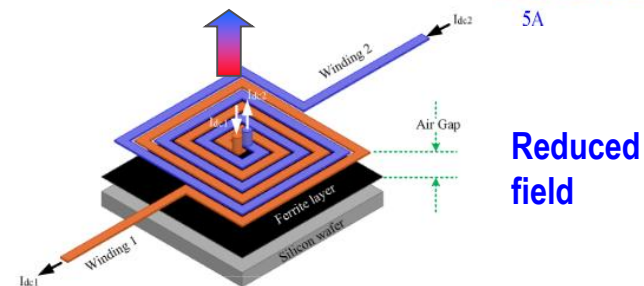
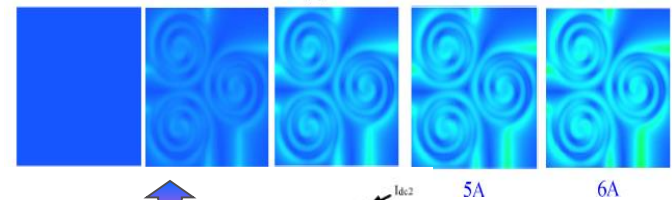
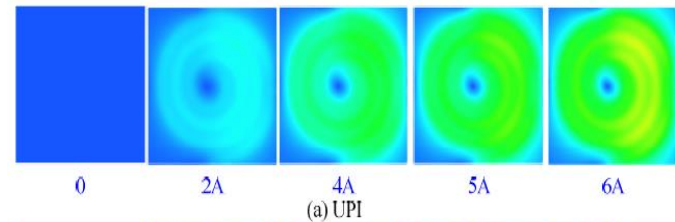
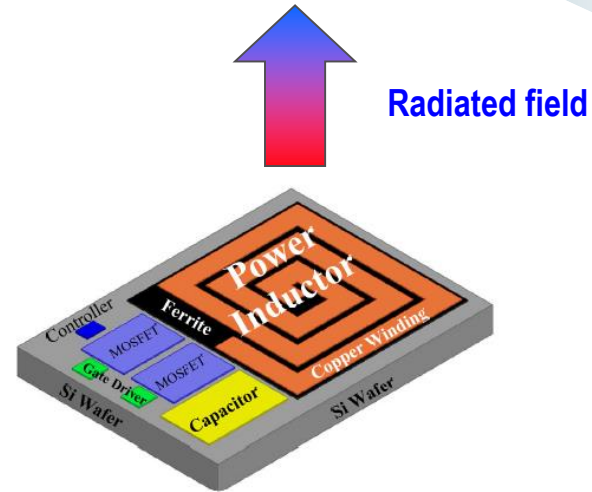
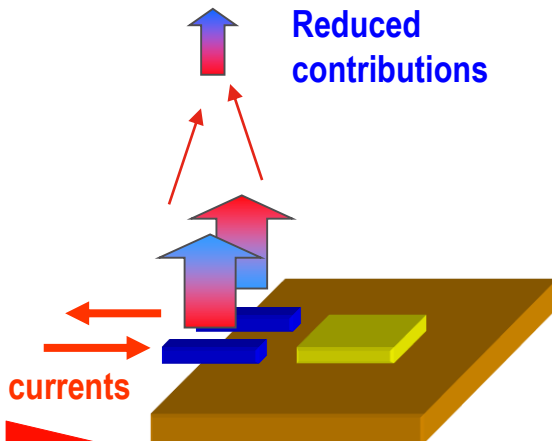
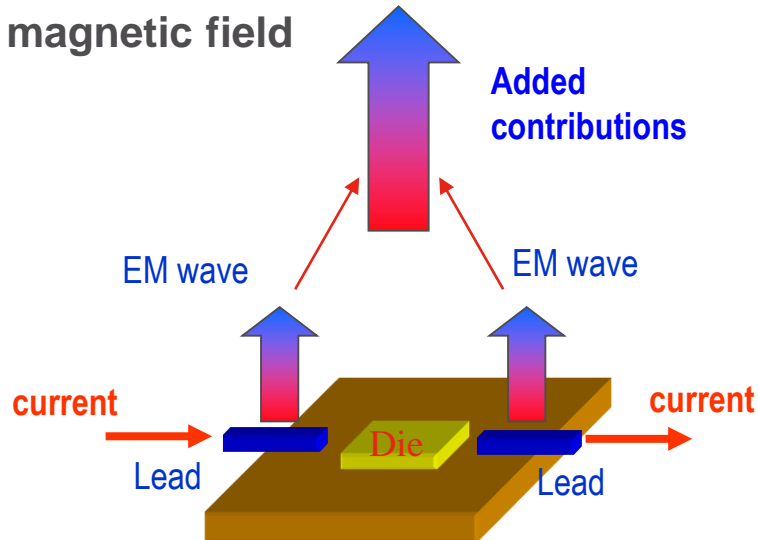


Many regions
devoid of returns



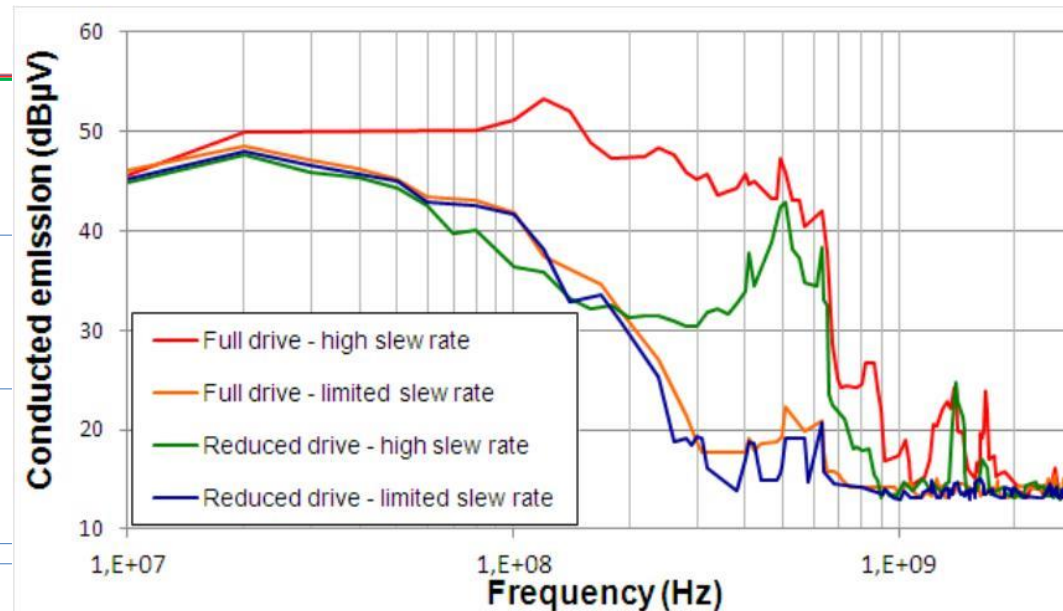
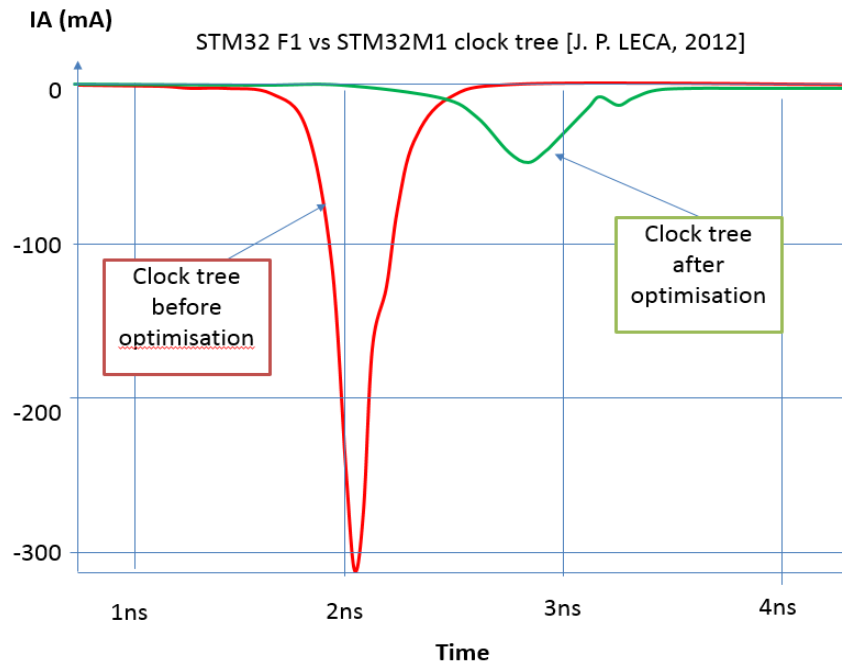
DESIGN GUIDELINES – CANCEL FIELDS

- Reduce current loops that provoke magnetic field



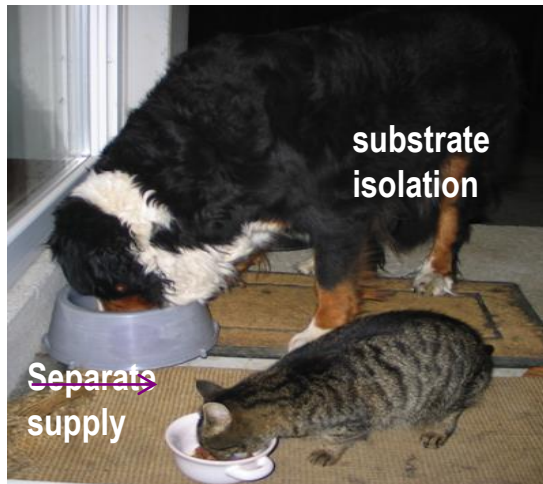
DESIGN GUIDELINES – REDUCE SWITCHING NOISE

- Reduction of clock buffer's drive
- Spread of the switching
- 20dB noise reduction
- Reduce drive, limit slew rate,
- Adapt impedance,
- Add local decoupling
- 20dB noise reduction

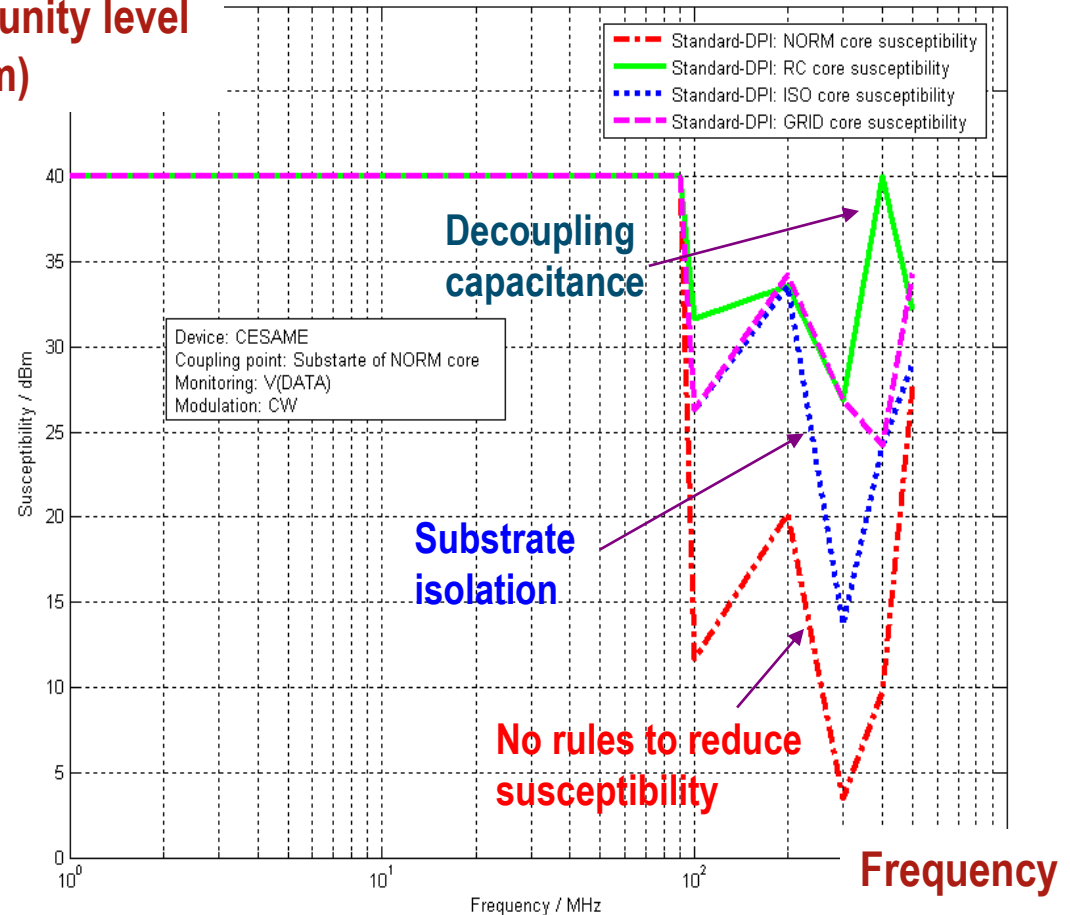


DESIGN GUIDELINES – ISOLATE AND DECOUPLE

- On-chip decoupling
- Resistive supply path
- Substrate isolation
- Separate supply
- Separation between incompatible blocks



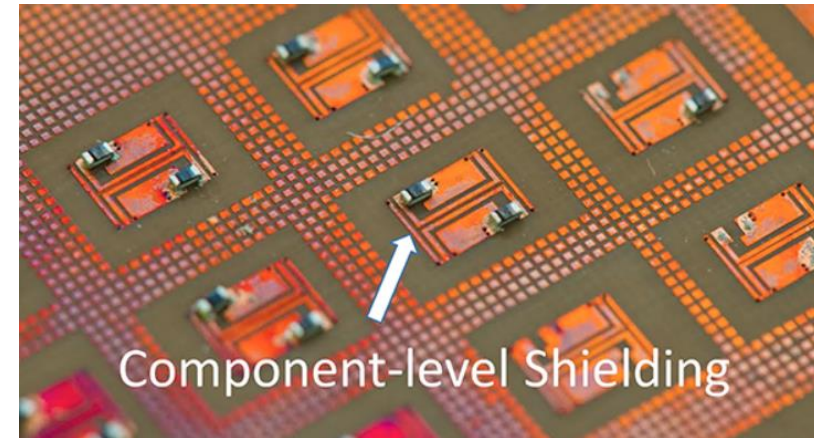
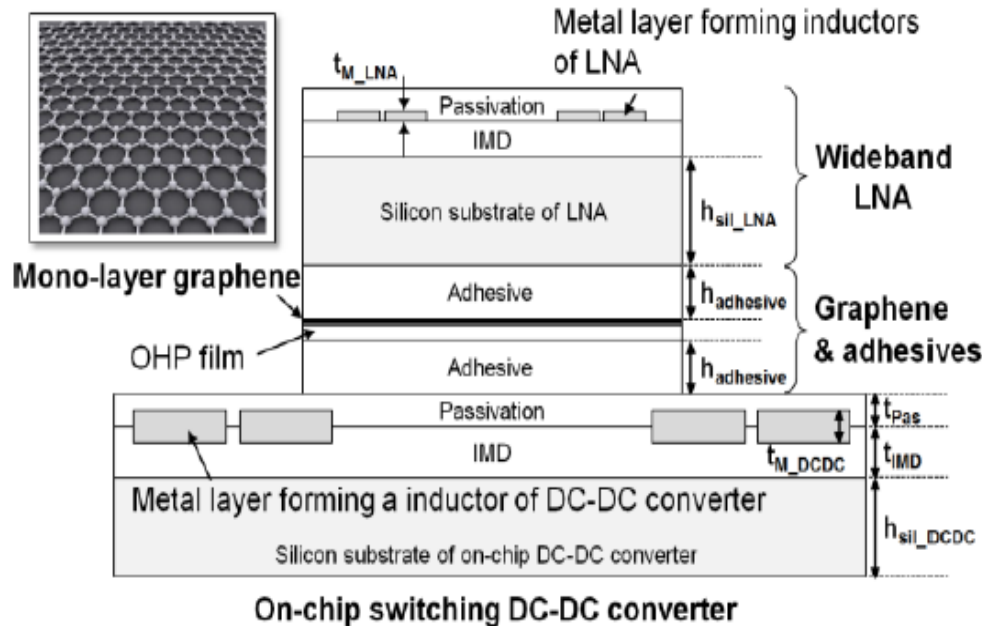
Immunity level
(dBm)



Work done at Eseo France
(Ali ALAELDINE)

- Graphene in stacked dies
- 10-15dB coupling reduction

- Thin magnetic-nonmagnetic multi-layered structure
- Trench-via array and multi-layered conductor structures (5G, 28-39 GHz)



<http://prc.gatech.edu/hg/item/585164>

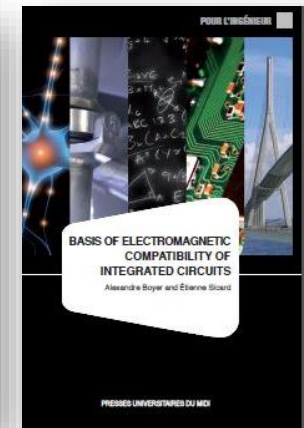
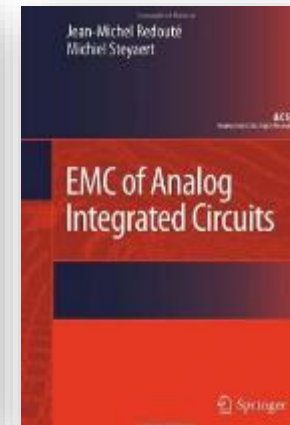
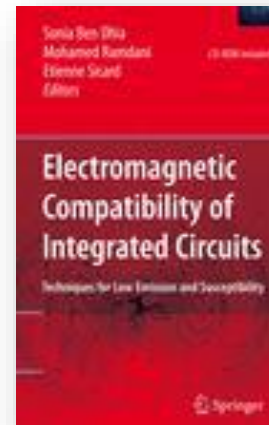
K. Kim, "Graphene-based EMI Shielding for Vertical Noise Coupling Reduction in 3D Mixed-Signal System", 2012



CONCLUSION

CONCLUSION

- The electronic market growth should be driven by 5G mobile, automatic drive, Internet of Things, etc.
- The trends towards nano-CMOS have been illustrated
- EMC concerns in terms of noise margin, higher frequencies and IO bandwidth
- Design guidelines for improved EMC have been introduced



www.ic-emc.org

Thank you for your
attention

*Special thanks to
Prof. Norocel CODREANU,
CETTI*