EMC-Aware System Design - A focus on Integrated Circuits

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In this talk, we propose an overview of IC technology evolution towards sub-10nm nodes and 3D integration, and its consequences on EMC.

Global trends in terms of EM interference are proposed. A status of the available standards for measurement of emission and susceptibility of ICs, including potential extensions to 10-100 GHz, is given. We also address the modelling of EMC at integrated circuits, and discuss the specific role of IBIS and its recent evolution to address Multi-Giga-bit data links with non-ideal supplies. We review the most efficient design guidelines for improved EMC, which primarily target ICs but also contribute to the overall sub-system EMC performance.

The revolutionary 3D-IC technology and the design options for improved signal integrity for Multi-Gb links, as well as emission and immunity improvements, conclude the talk.