Through Silicon Vias Annealing: A thermo-mechanical assessment

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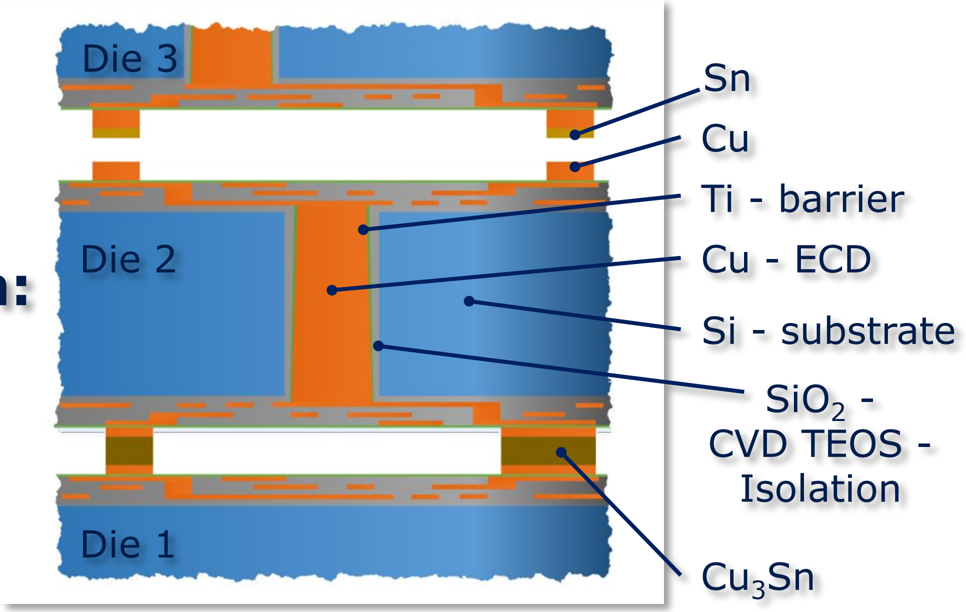
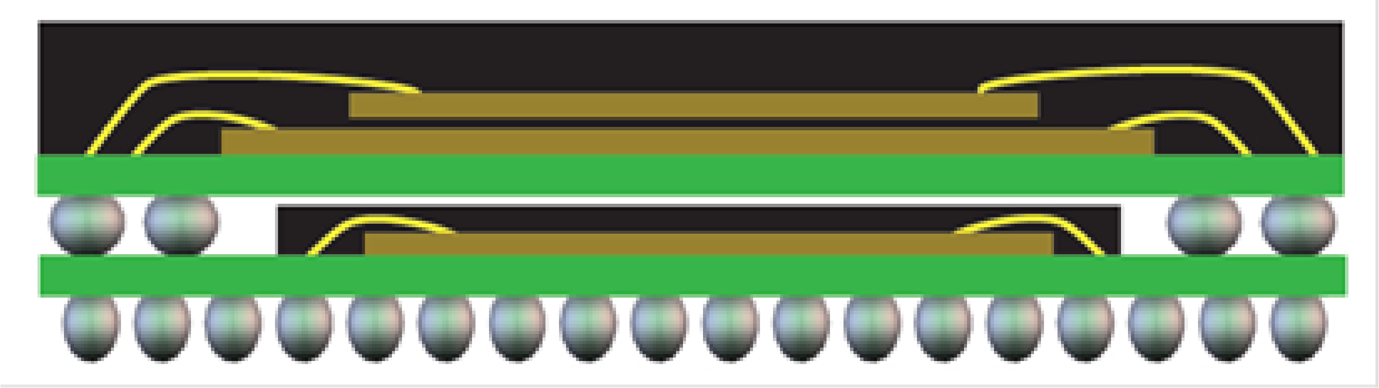
Bucuresti, October 24th 2014

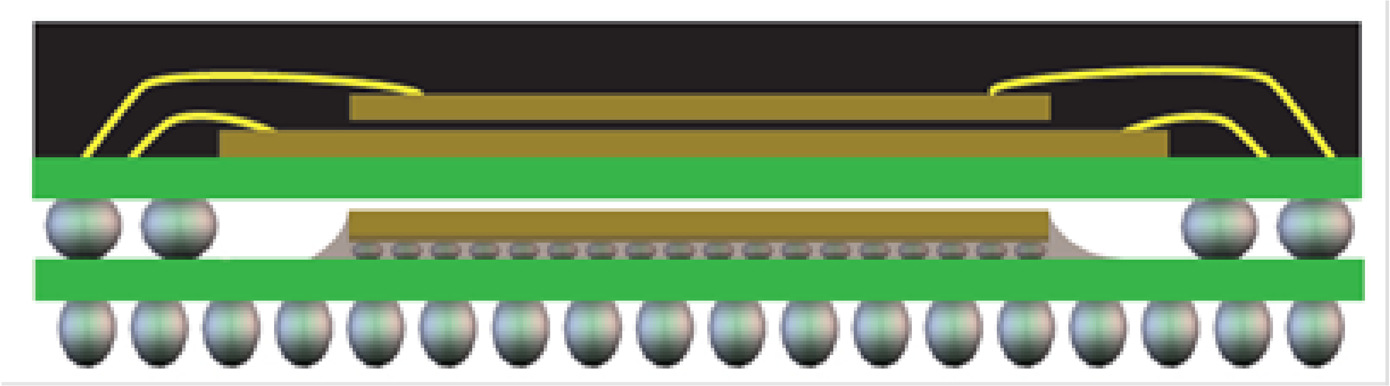
- **Introduction:**
  - 2,5 and 3D Integration
- **Motivation:**
  - TSV annealing aspects
- **Annealing characterization:**
  - die warpage
  - copper protrusion
  - EBSD on TSVs
- **FEM and µ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results



3D architecture including TSVs

Introduction: Package on Package





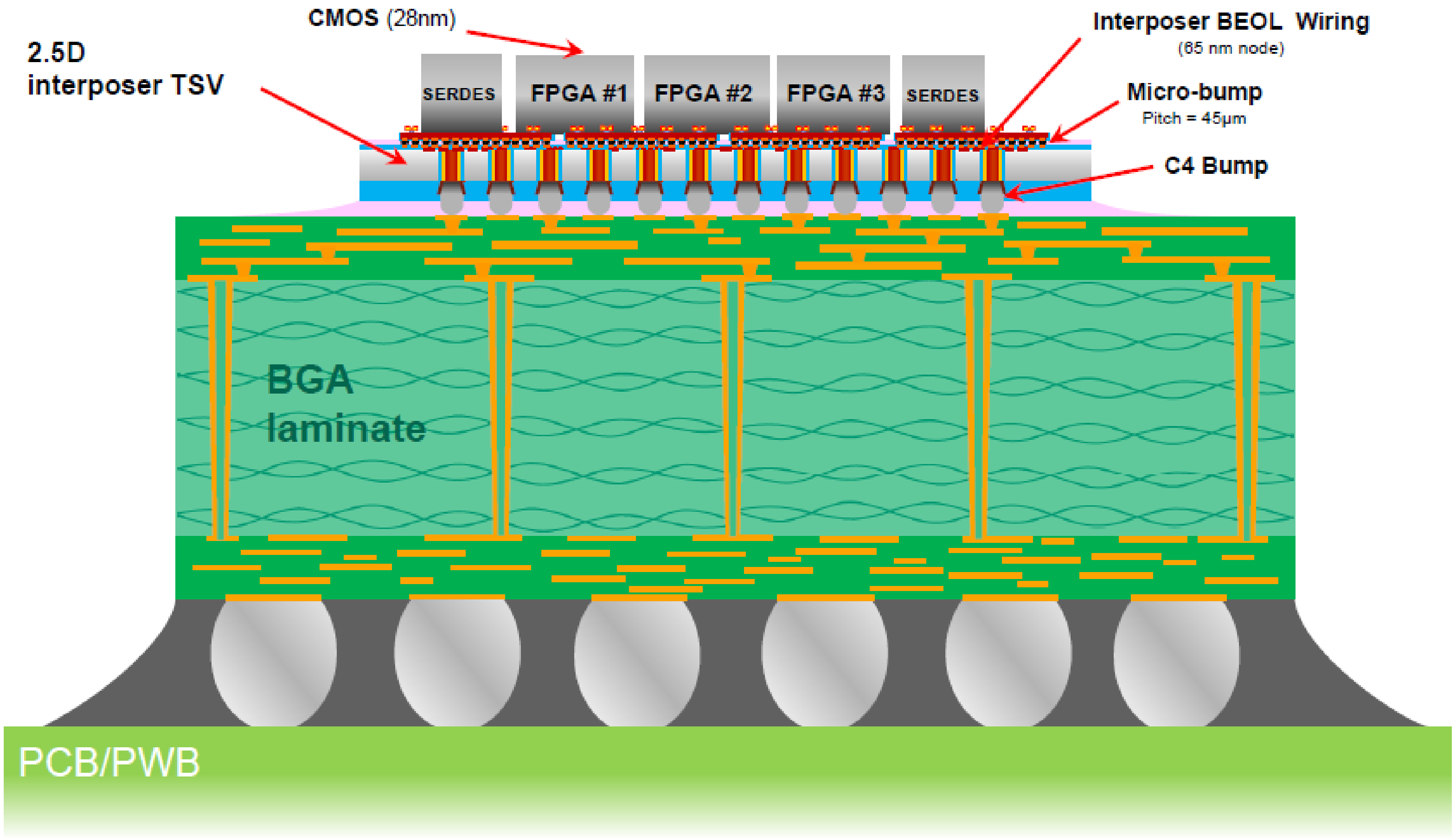
Source: Yole 2012

Introduction: 2,5D vs. 3D-Integration

	several standard packages	2.5D SiP	3D SiP
Technology and infrastructure maturity	+	-	--
Electrical bandwidth	-	+	++
Power consumption	-	+	+
Heterogeneous integration	-	+	+
Size	-	+	++
Thermal Management	++	+	-

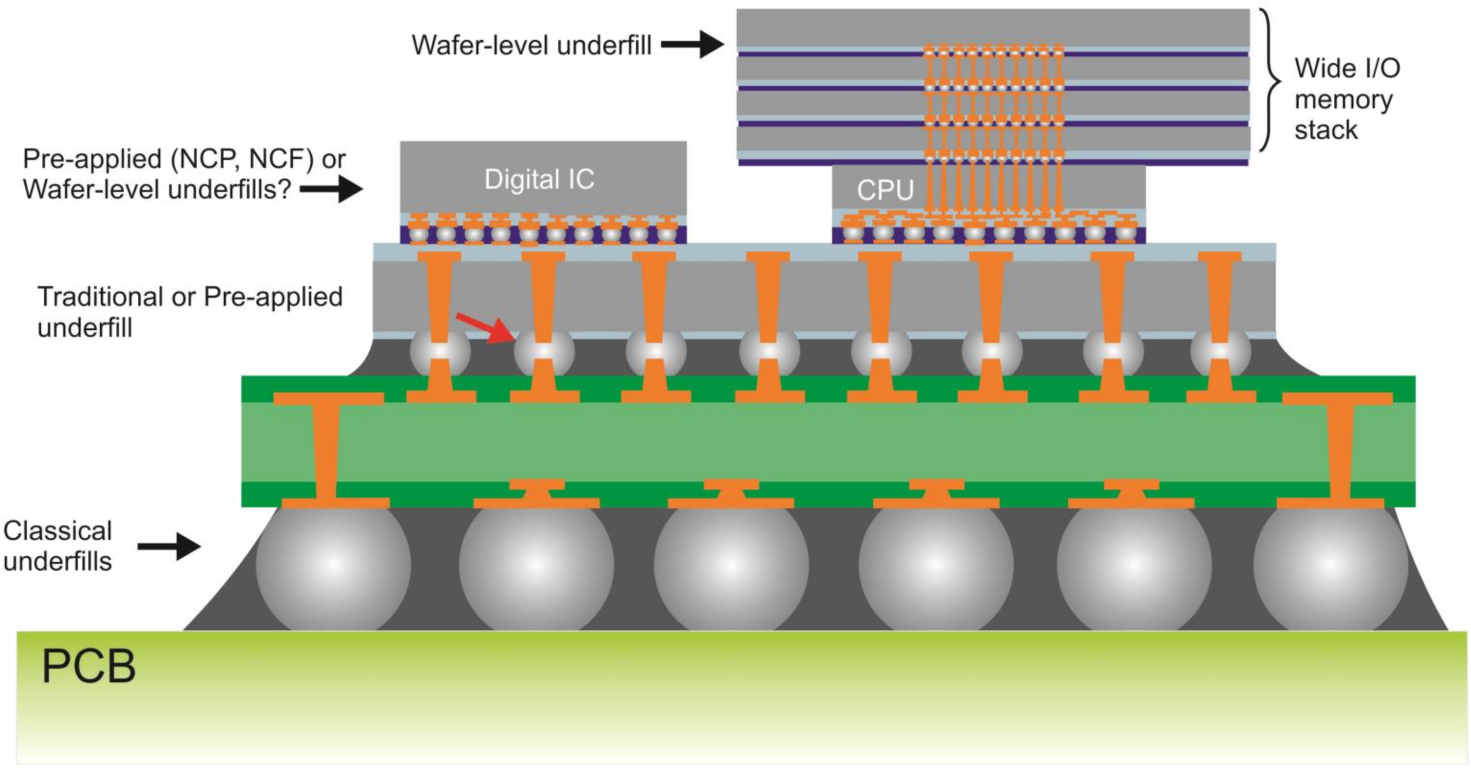
Source: Yole 2012

Introduction:2,5D Integration



Source: Yole 2012

Introduction: 2,5D und 3D Integration



Source: Yole Polymeric materials 2012

Introduction:TSV - dimensions

Typical diameters: 5-20 µm

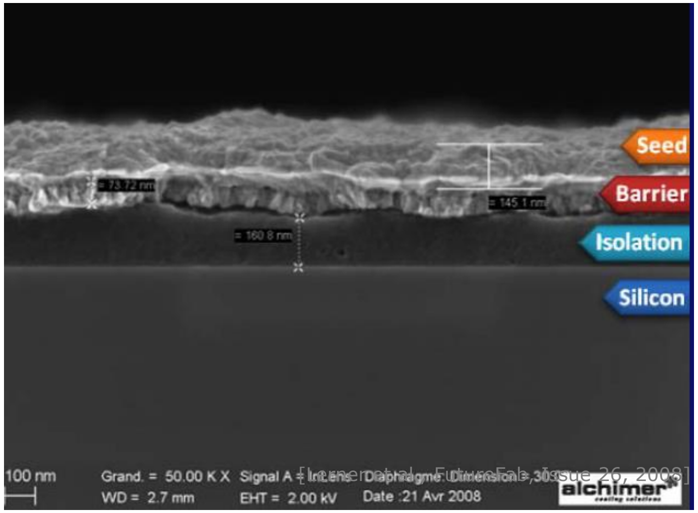
Aspect ratio: up to 1:10

TSV-layers

Isolation (SiO_2) 400 nm

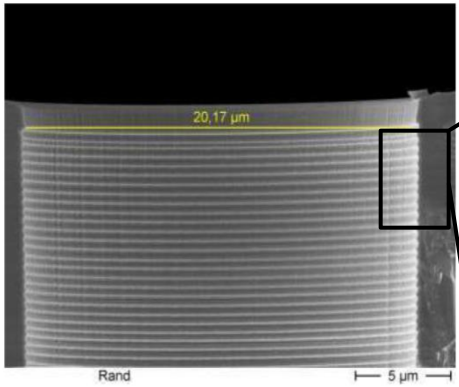
Barrier-Layer (Ta/TaN) respectively 80 nm

Seed-Layer (Cu) 600 nm



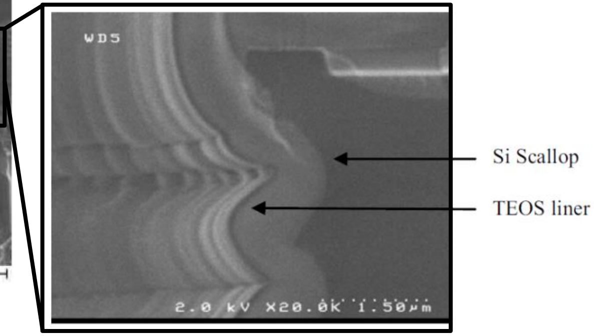
[Lerner et al., FutureFab, Issue 26, 2008]

Etched Si (Bosch process)



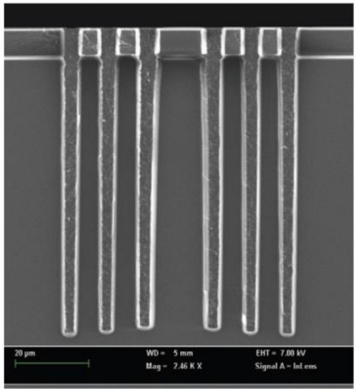
[Wolf et al., ESTC, 2010]

Scallops in Si and SiO_2-isolation layer



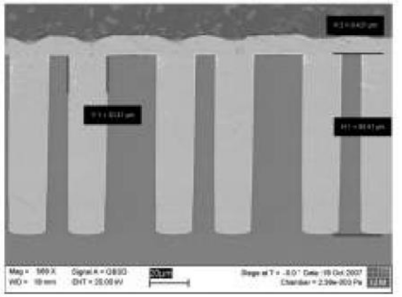
[Powel et al., IITC, 2008]

unfilled TSVs (d=5µm)



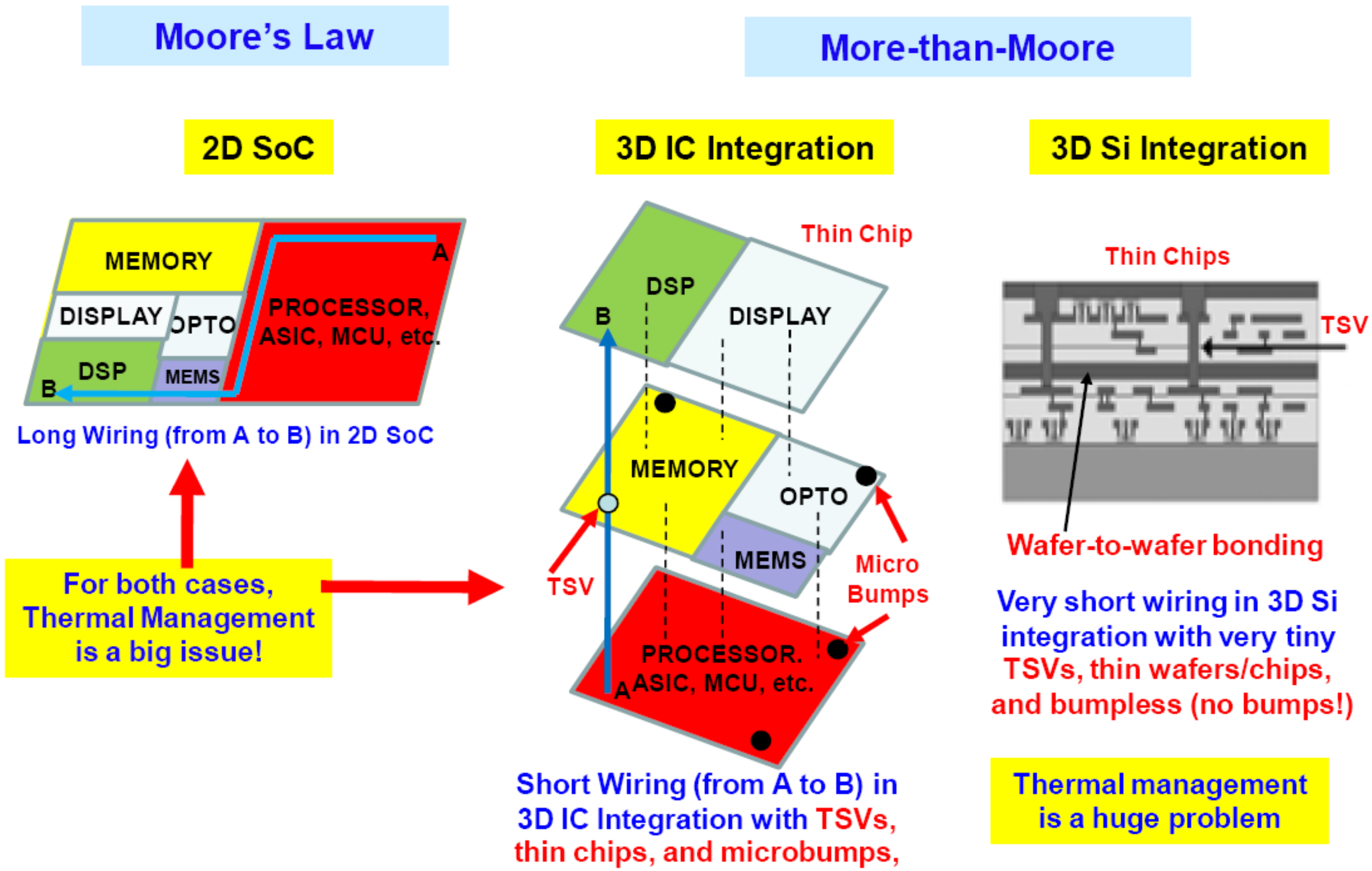
[Laviron et al., ECTC, 2009]

Cu-filled TSVs (d=20µm)

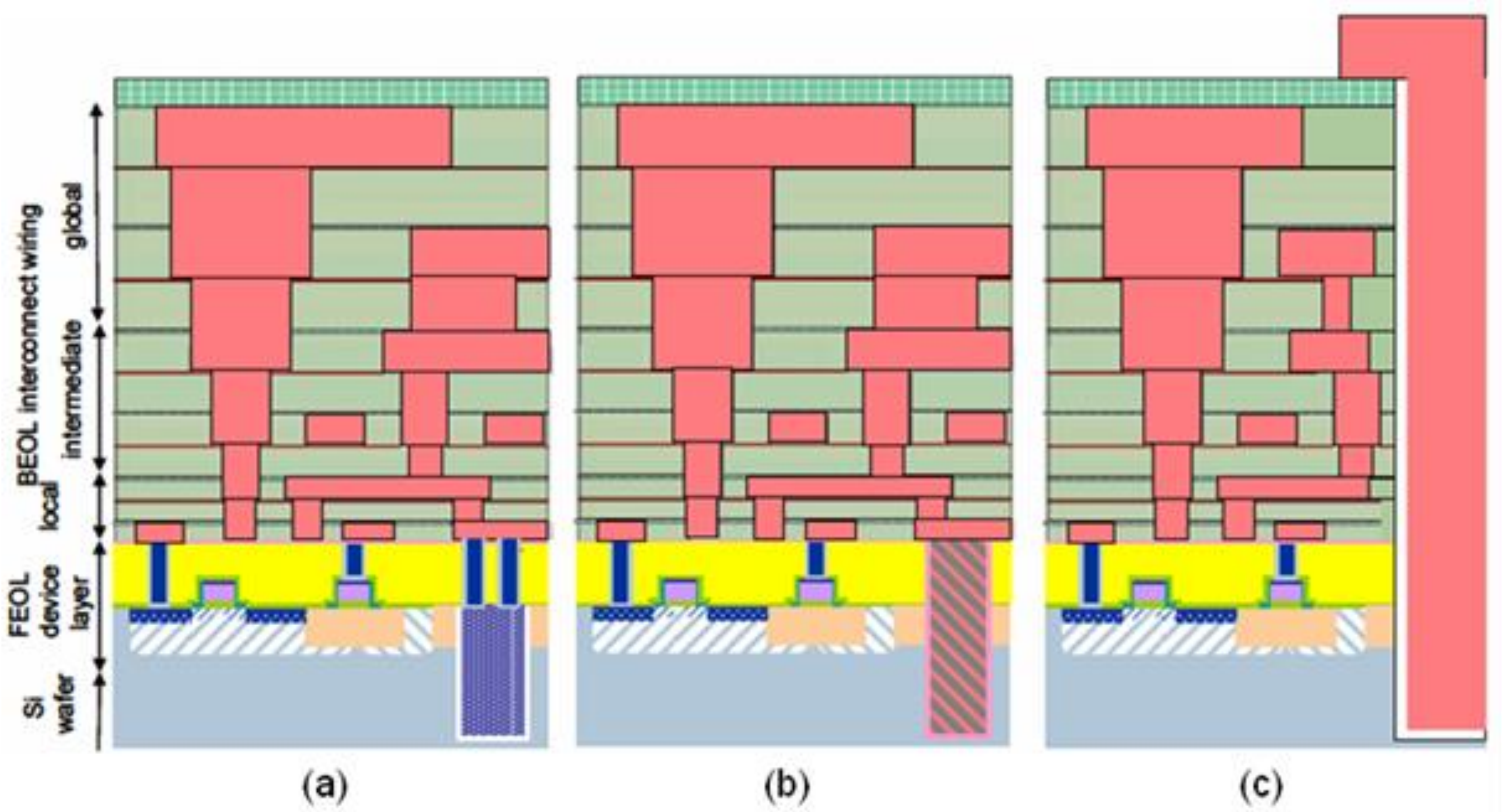


[Wolf et al., ESTC, 2010]

Moore's Law vs. More-Than-Moore



[Lau, ECTC, 2010]



a) Via first

TSV->Thinning-> CMOS

b) Via middle

CMOS->TSV->Thinning

c) Via last

CMOS->Thinning->TSV

Source: Yole 2012

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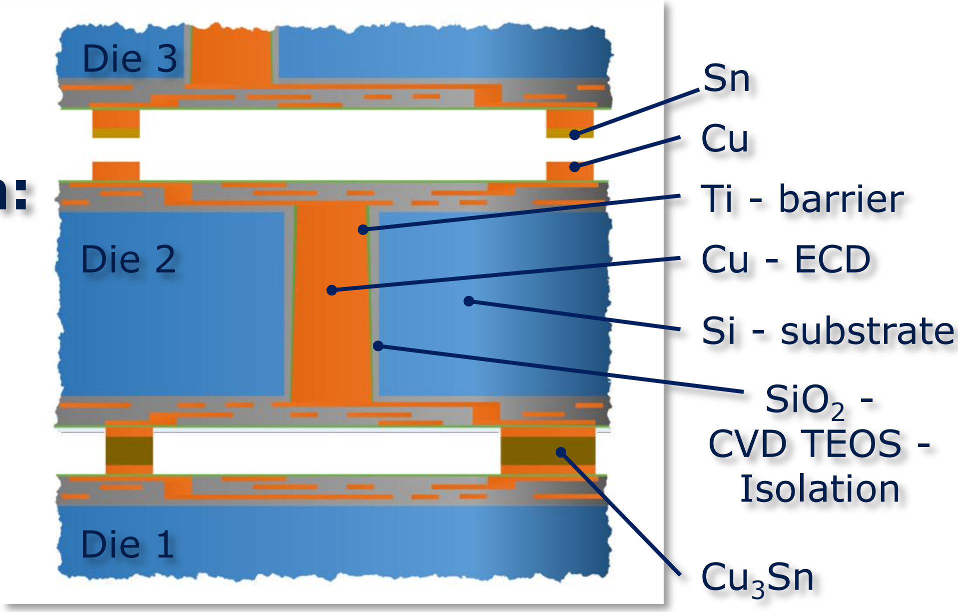
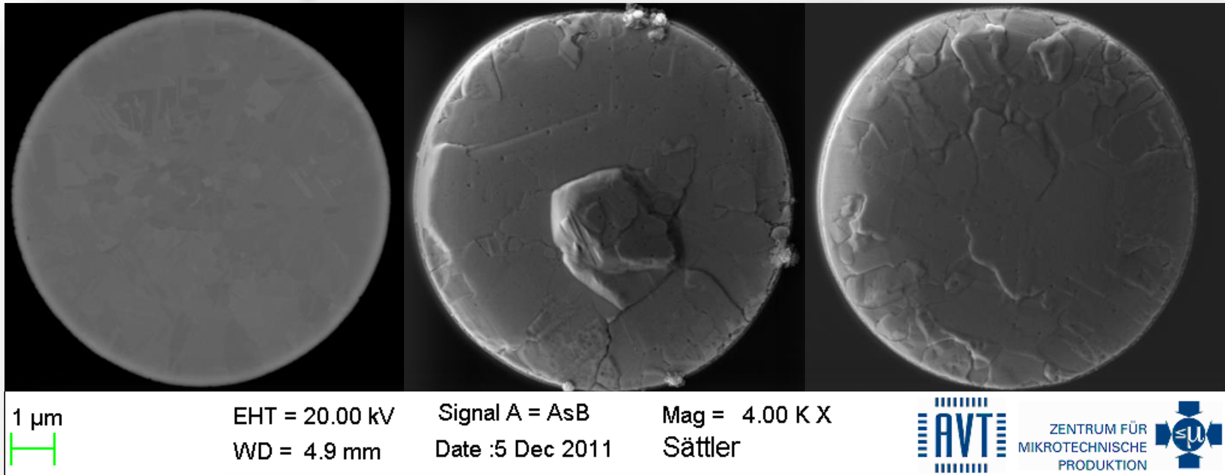


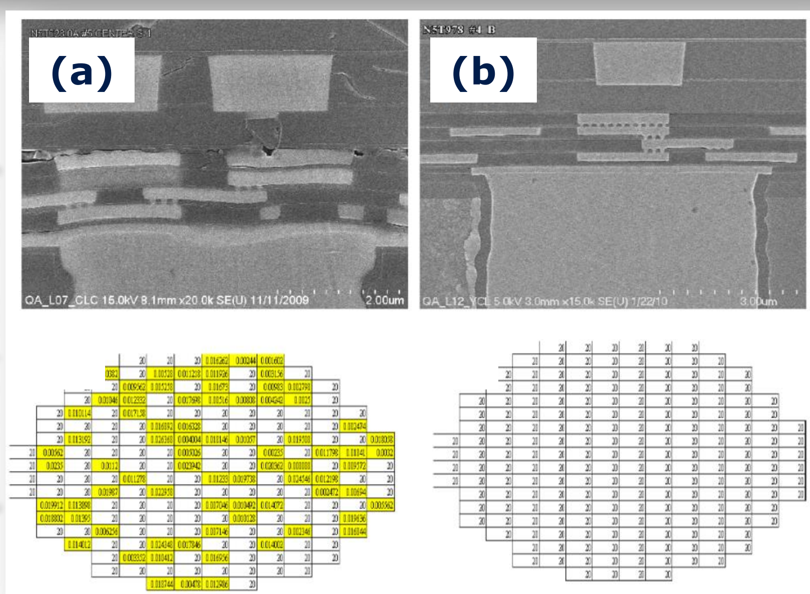
3D architecture including TSVs

Motivation: Copper Protrusion

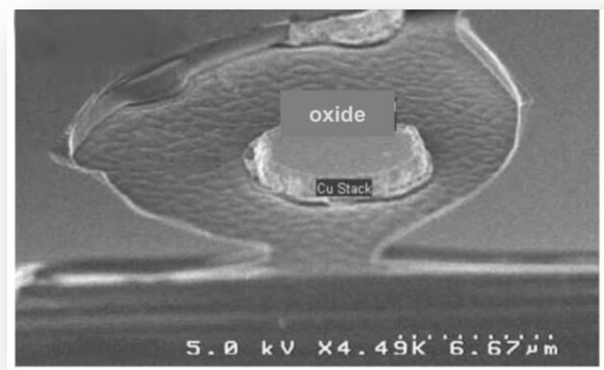
w/o annealing *annealing (0,5h/450°C)*



- layer cracking and delaminations due to copper protrusion



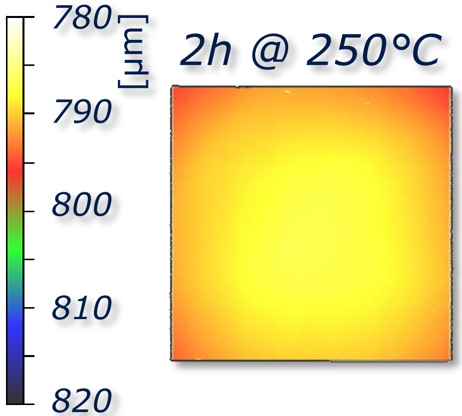
[Lin et. al., IEDM 2010]

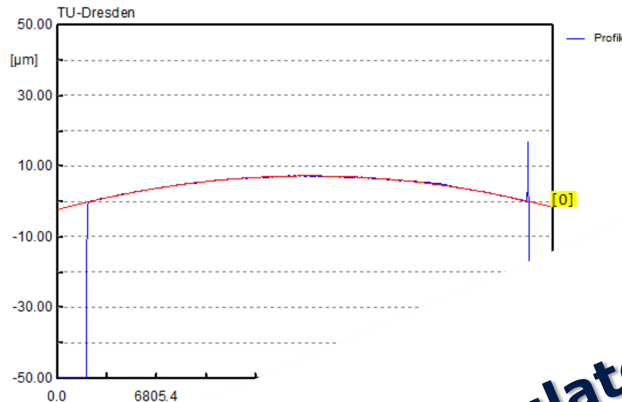


[Lu et. al., Thermo-mechanical Reliability Challenges of 3D Interconnects]

Motivation: stresses caused by TSV fabrication

- die/wafer warpage

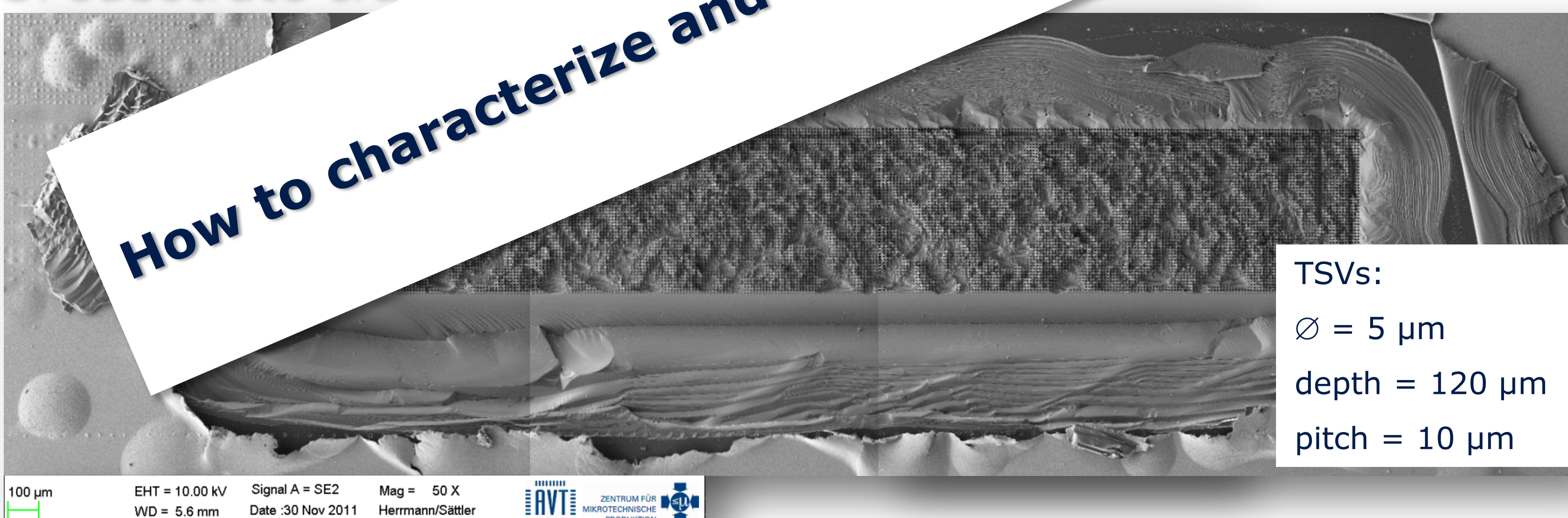




- degradation of device performance

[Mercha et. al., IEDM 2010]

- Si substrate cracki



TSVs:

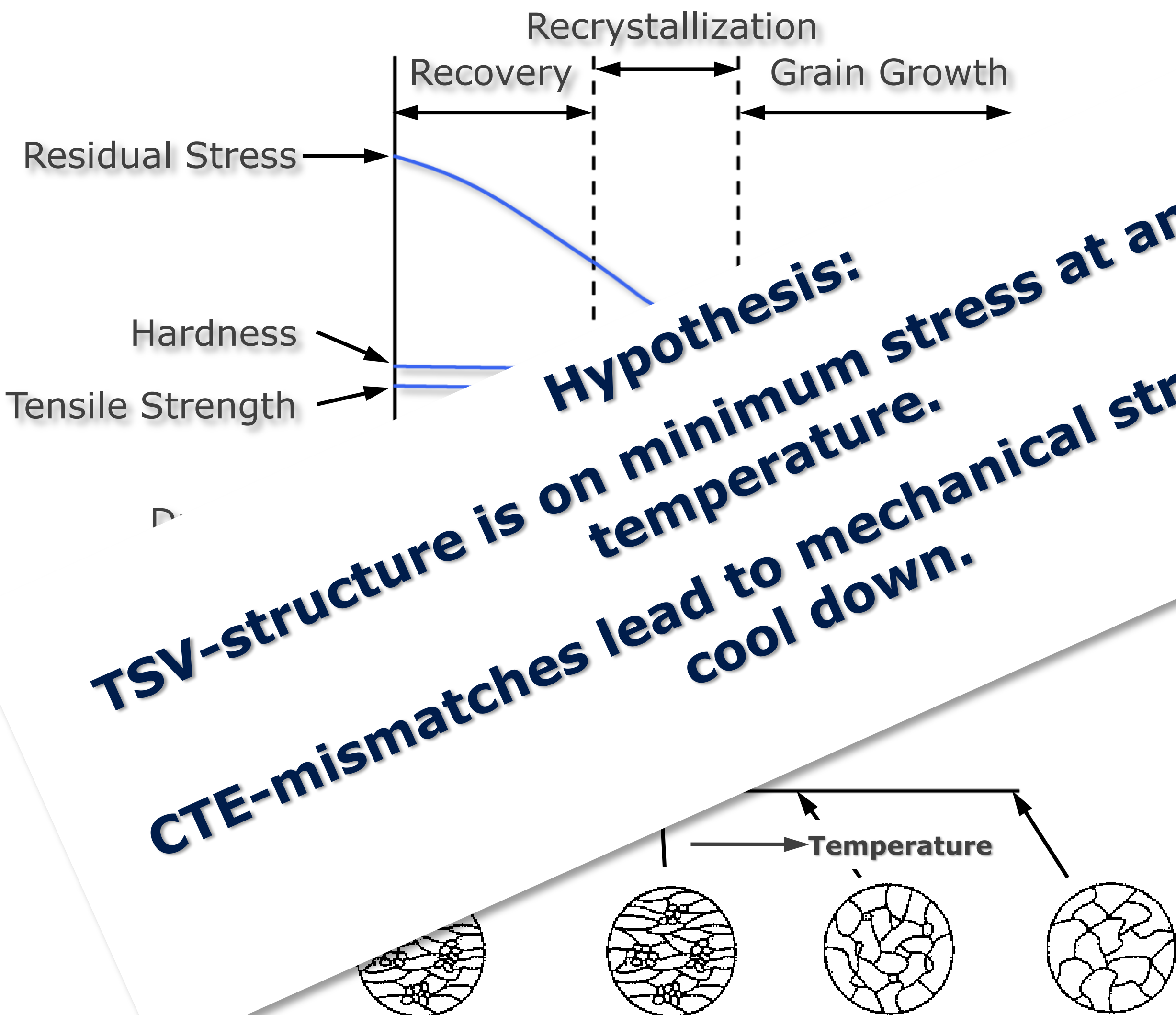
∅ = 5 µm

depth = 120 µm

pitch = 10 µm

How to characterize and calculate stresses in silicon?!

Motivation: Annealing behavior of Copper



Hypothesis:

TSV-structure is on minimum stress at annealing temperature.

CTE-mismatches lead to mechanical stress during cool down.

°C

per:

- unstable material behavior
- decrease of crystallographic defects and residual stresses
- grain growth

[Materials Science for Engineering Students; Traugott Fischer; 2009]

[Werkstoffkunde für Ingenieure; Eberhard Roos; 2008]

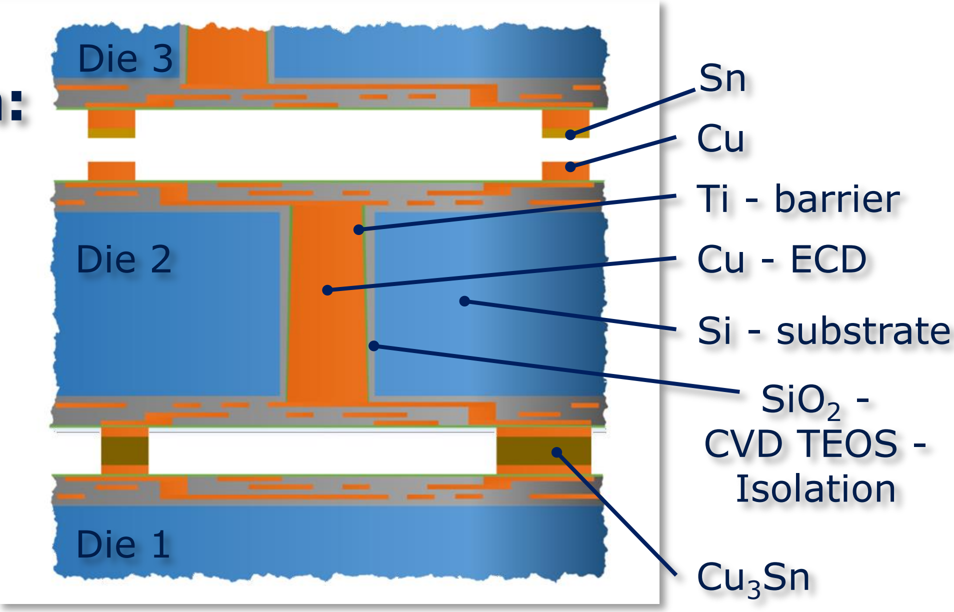
proof of hypothesis by experiment and simulation

- perform annealing with supplementary characterization
- search for increased warpage, protrusion and grain growth indicating coppers annealing behavior
- measure stresses using Raman spectroscopy

- implement simulation model using hypothesis assumptions
- stress free at annealing temperature
- cool down to room temperature as thermal load

compare measured and calculated stresses

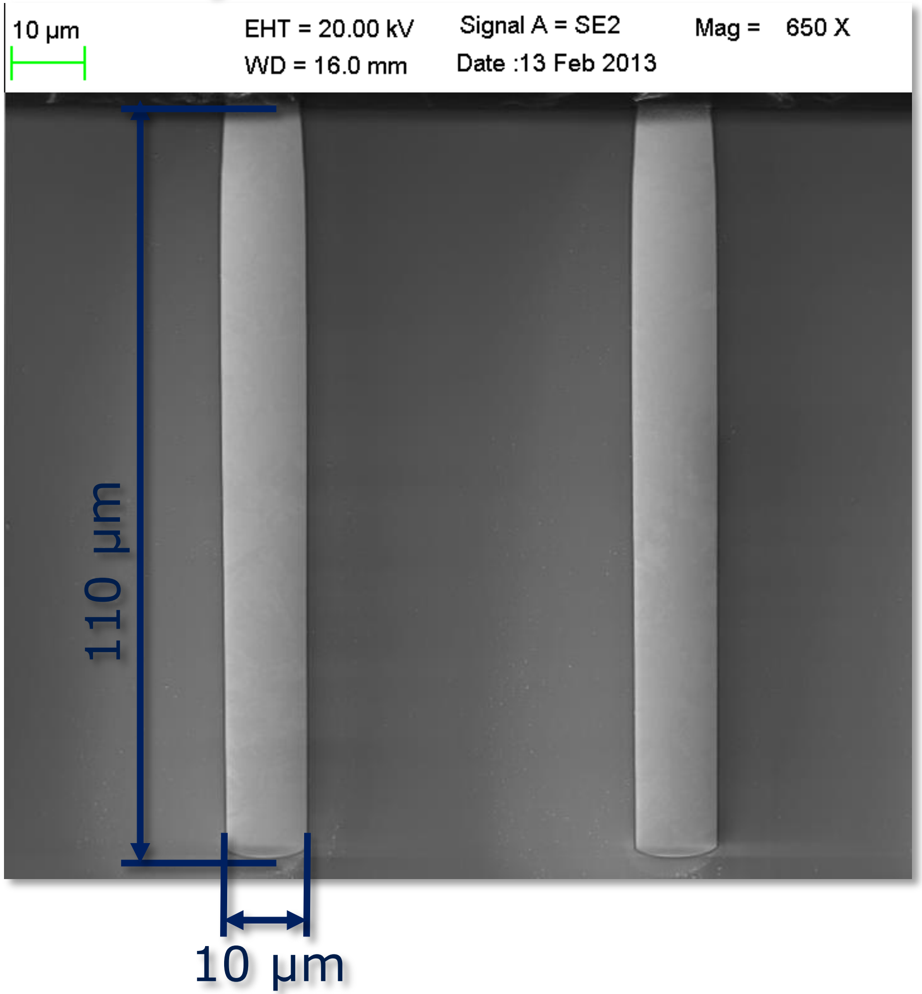
- **Annealing characterization:**
  - die warpage
  - copper protrusion
  - EBSD on TSVs
- **FEM and µ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results



3D architecture including TSVs

Experimental: Test samples

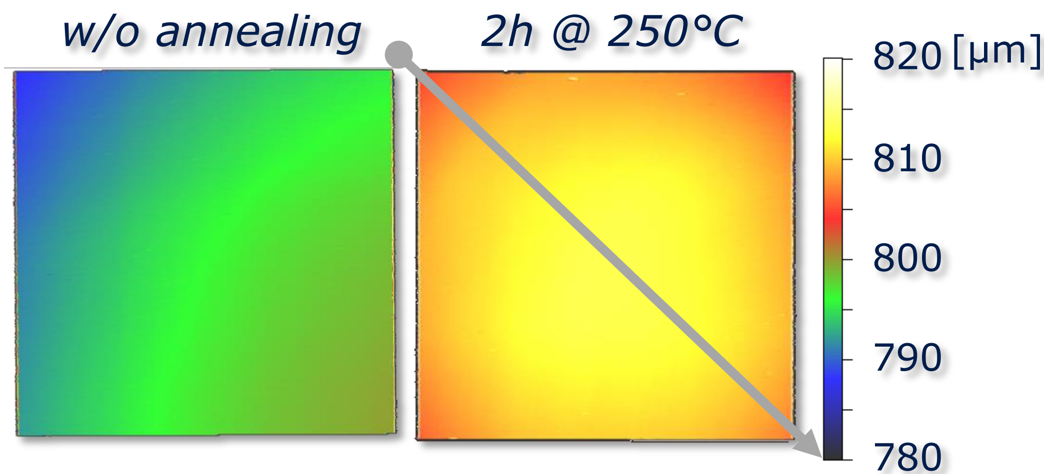
SEM image of the examined TSV structures



- die samples:
  - 3 cm x 3 cm x 700 µm
  - samples taken after copper fill and overburden CMP (unthinned die)
  - 600 nm SiO_2 on top
  - TSV-pitch 55 µm
- experimental:
  - annealing conditions:

    T: 250 °C
    t: 2 h
- measurement:
  - warpage
  - grain structure
  - copper protrusion
  - µRS

- measurement of die warpage:



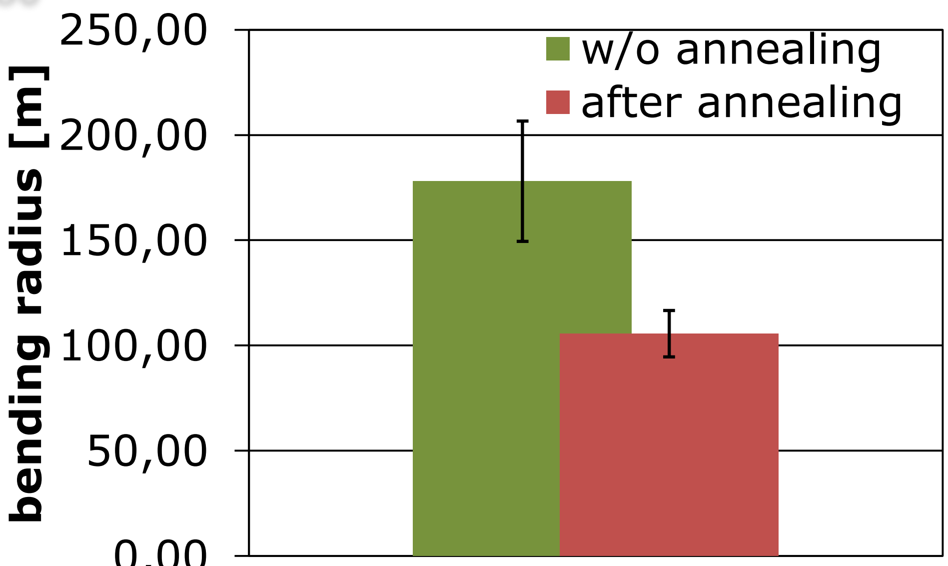
height map of the test die back sides

- confocal sensor
- creation of height maps
- evaluation of diagonals bending radii

→ bending even without annealing

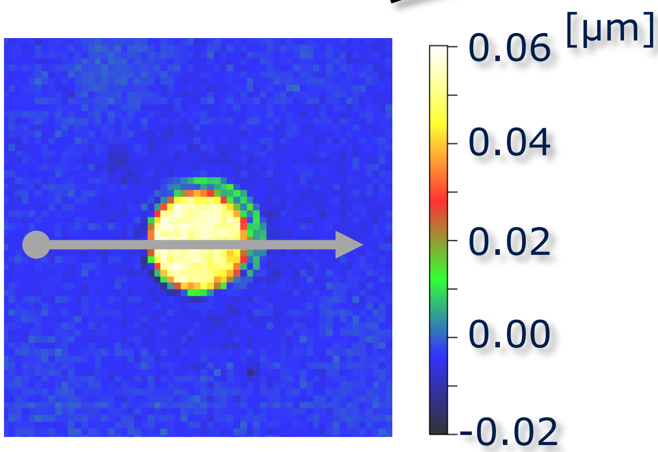
→ increased warpage after annealing (decreased bending radius)

→ stress increase

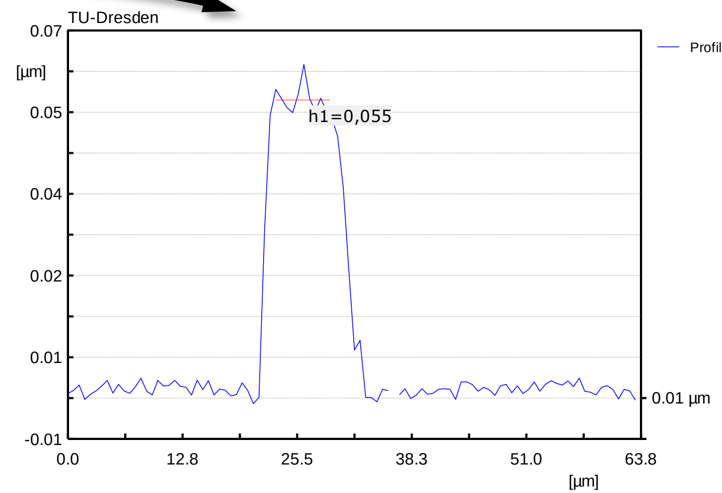


Experimental: Copper Protrusion

- measurement of copper protrusion:



height map of a TSV's copper protrusion

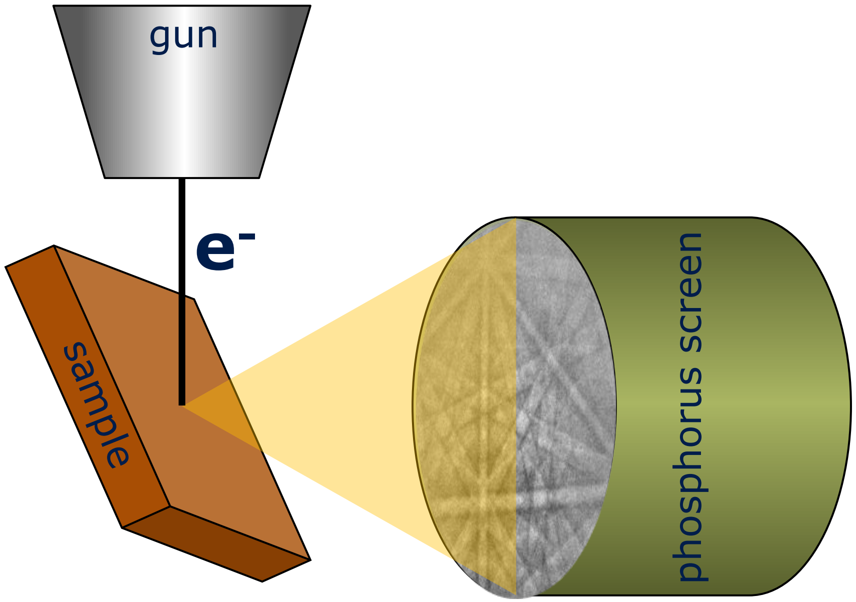


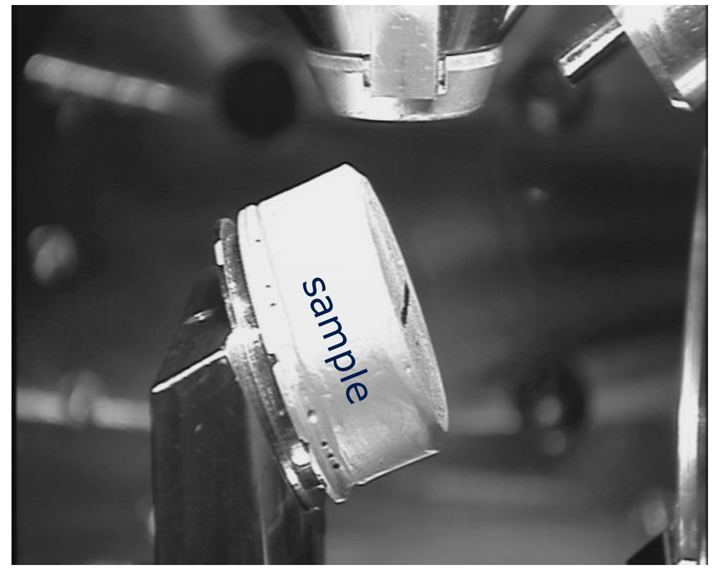
height profile and measured copper protrusion

- confocal microscopy
- creation of height maps
- evaluation of TSV profiles average heights

→ copper protrusion: 61 ± 4 nm in average

Electron BackScatter Diffraktion – experimental arrangement and functional principle:

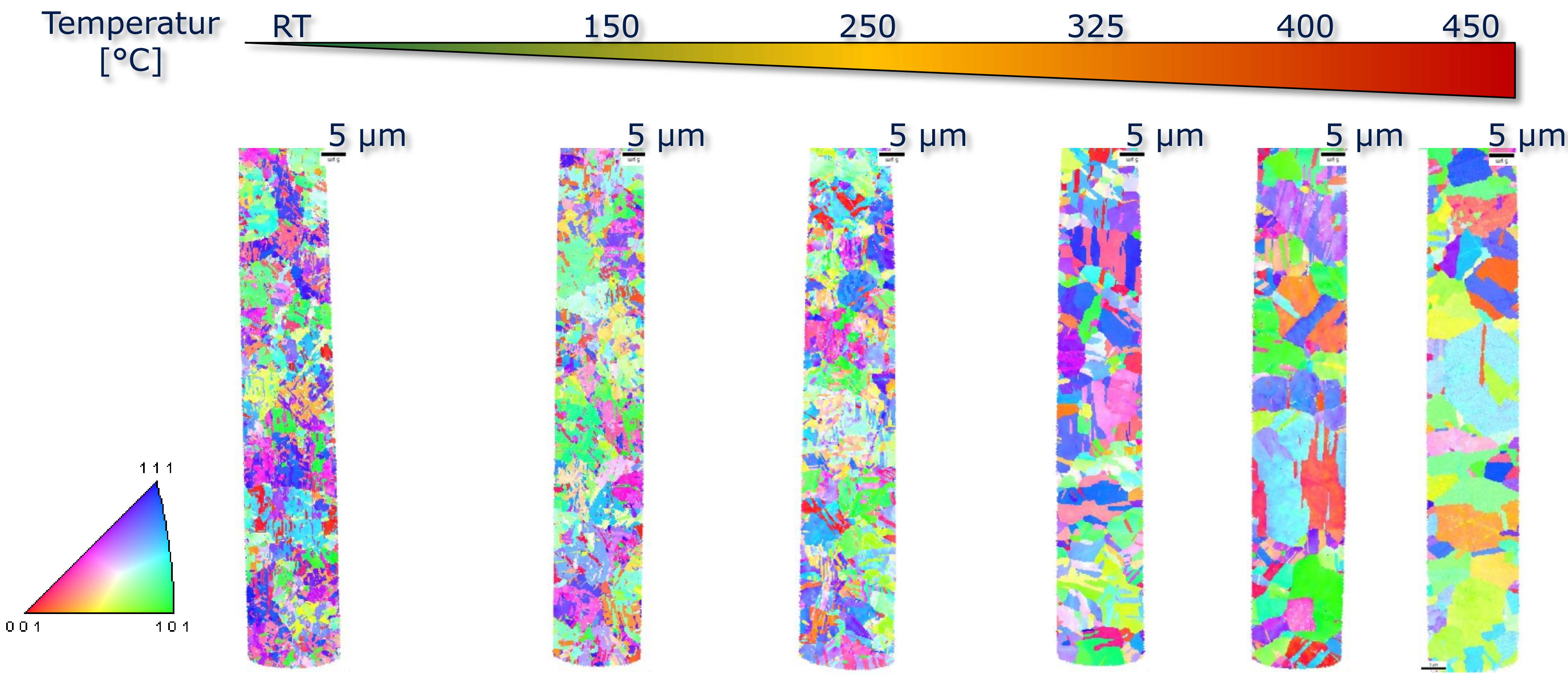




- Sample with an angle of 70° inside the SEM
- Incident electron beam scatters inelastic on lattice atoms
- Bragg conditions → constructive interference (diffraction pattern – Kikuchi-pattern)
- CCD camera records pattern from phosphorus screen

Evolution of crystal structure as result of annealing

- comparison of grain structures after 4 h annealing:

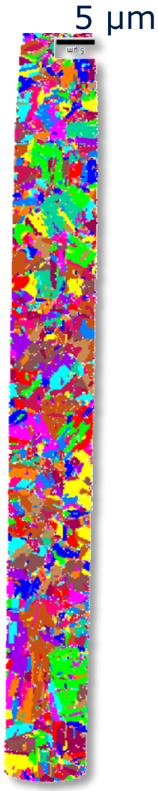


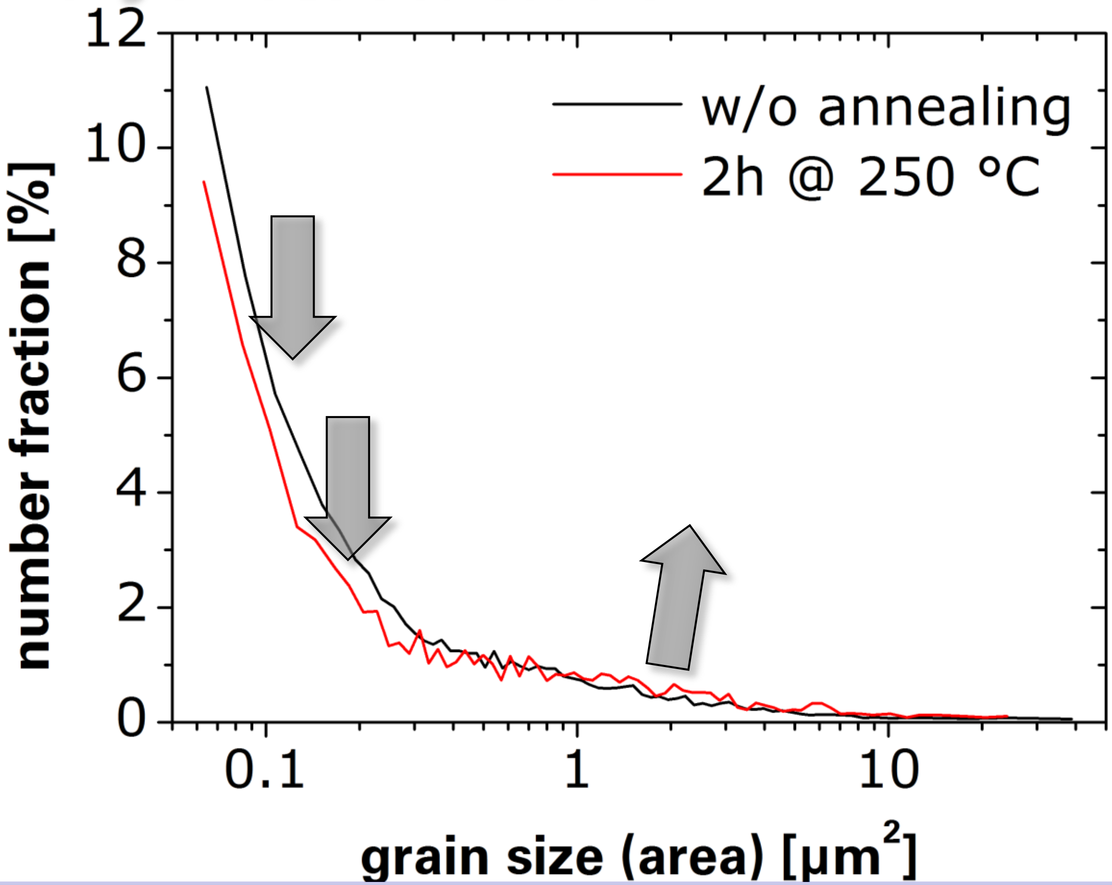
→ annealing above recrystallization temperature creates grain growth

Grain growth as a result of annealing

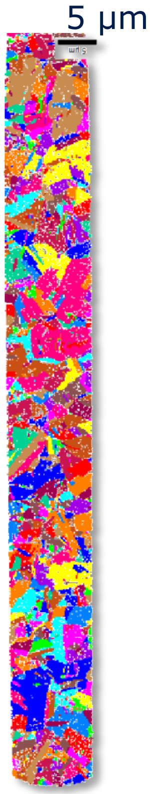
- comparison of grain size distributions:

RT





250°C/2h



→ initiated grain growth
→ only marginal grain size changes measured → additional evaluation of twin boundaries as crystallographic defects

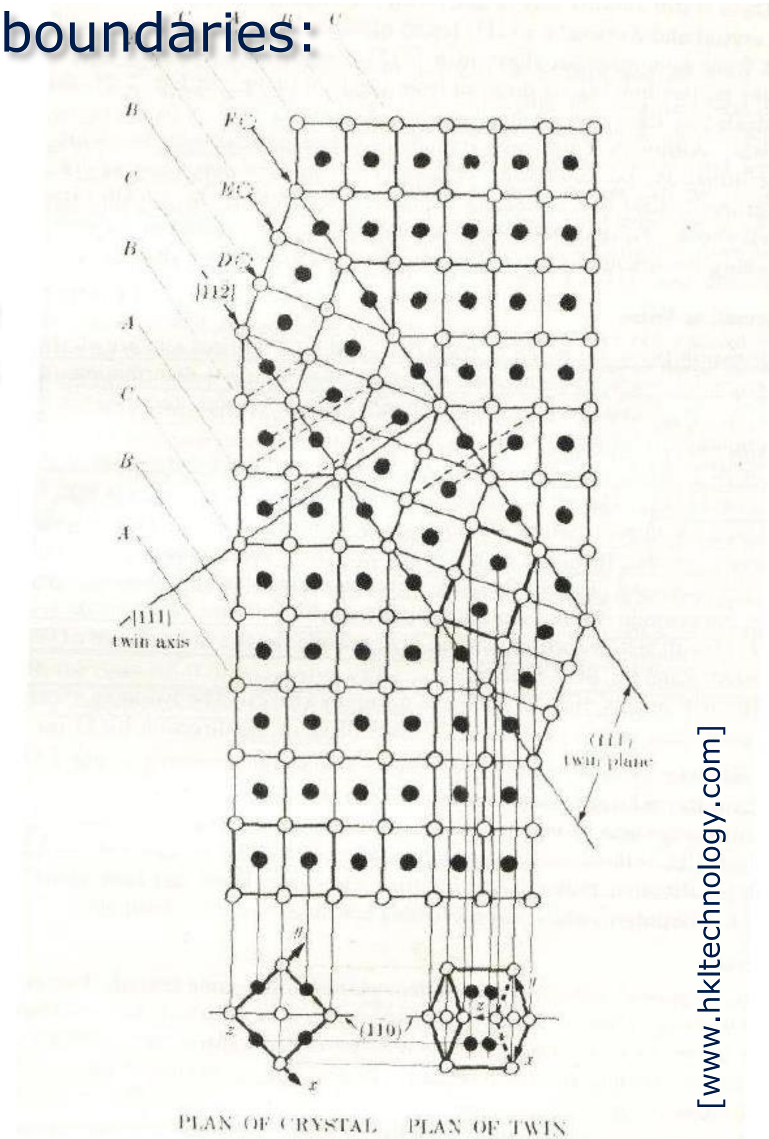
Evolution of crystal structure as result of annealing

- Misorientations between grains / twin boundaries:

w/o annealing

- CSL – coincident site lattice
- CSL boundary - some of the atoms in two crystal lattices separated by the boundary are coincident
- typical twin boundaries of copper:

Σ Type	Angle	Axis
Σ3	60°	111
Σ9	38.94°	110
Σ27a	31.59°	110
Σ27b	35.43°	210

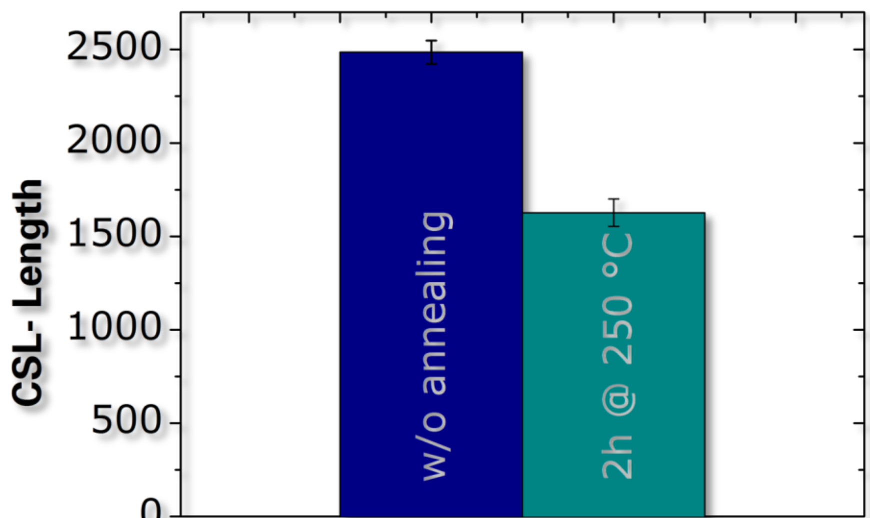


[www.hkltechnology.com]

- Misorientations between grains / twin boundaries:

CSL	w/o annealing	2h @ 250°C
Σ	Length [µm]	Length [µm]
3	2230±52	1427±63
9	233±9	153±7
27a	37±1	26±2
27b	51±3	20±2

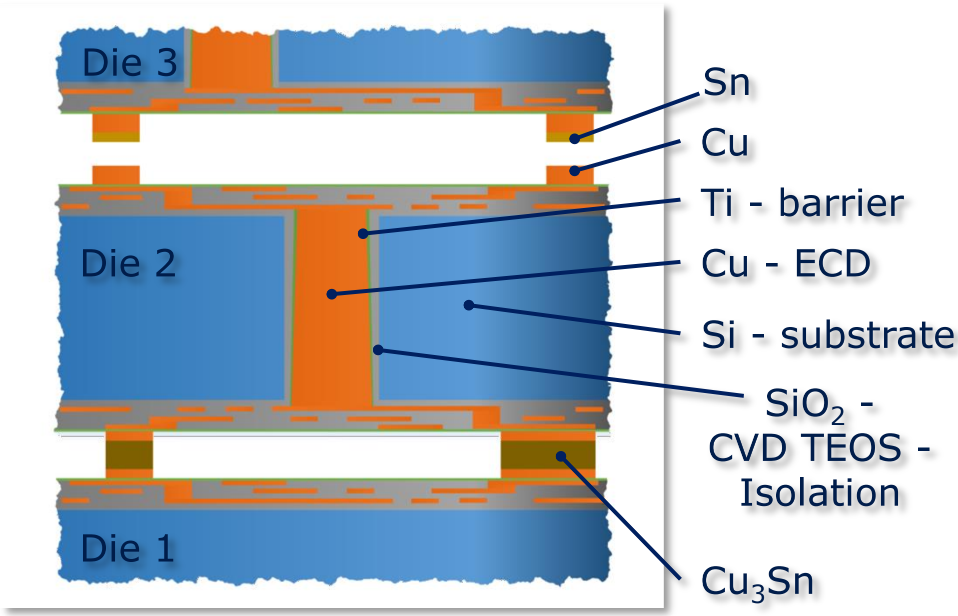
w/o annealing



2 h @ 250°C

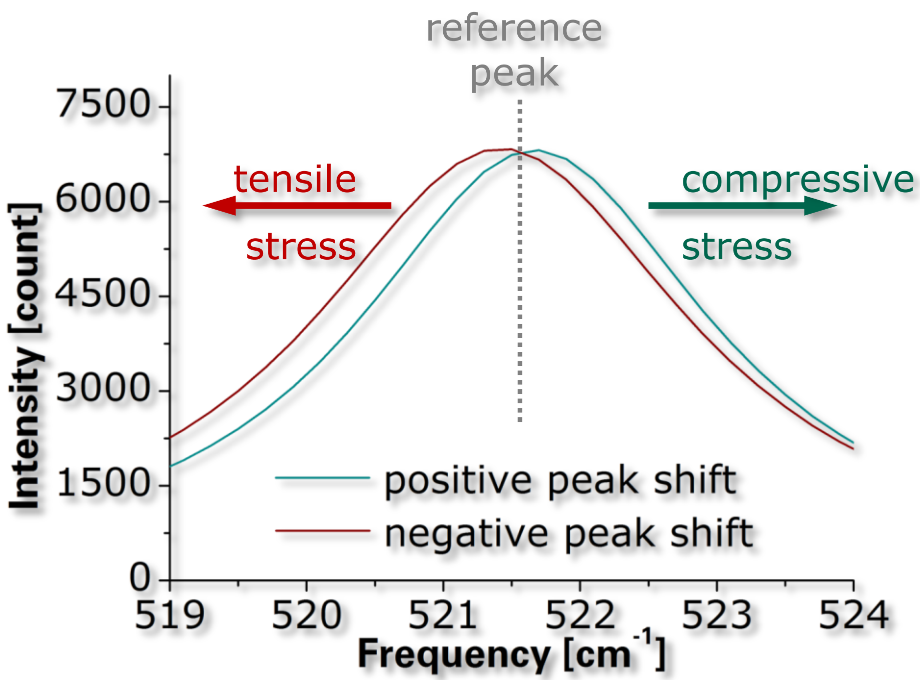
→ decreased crystallographic defects due to annealing

- **FEM and µ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results



3D architecture including TSVs

- Raman spectroscopy for stress measurement:



- strains effect Raman peaks

→ uniaxial stress model:

positive shift - compression

negative shift - tension

- **BUT**: peak position is dependent on all strain tensor elements

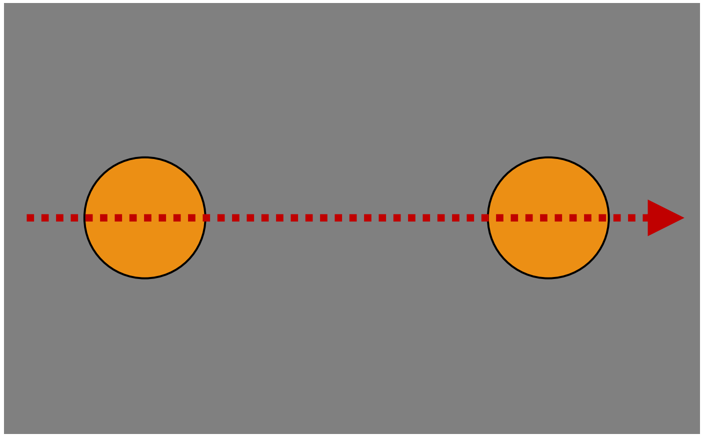
→ general stress calculation rule needed

- conversion of strains into Raman Shifts:

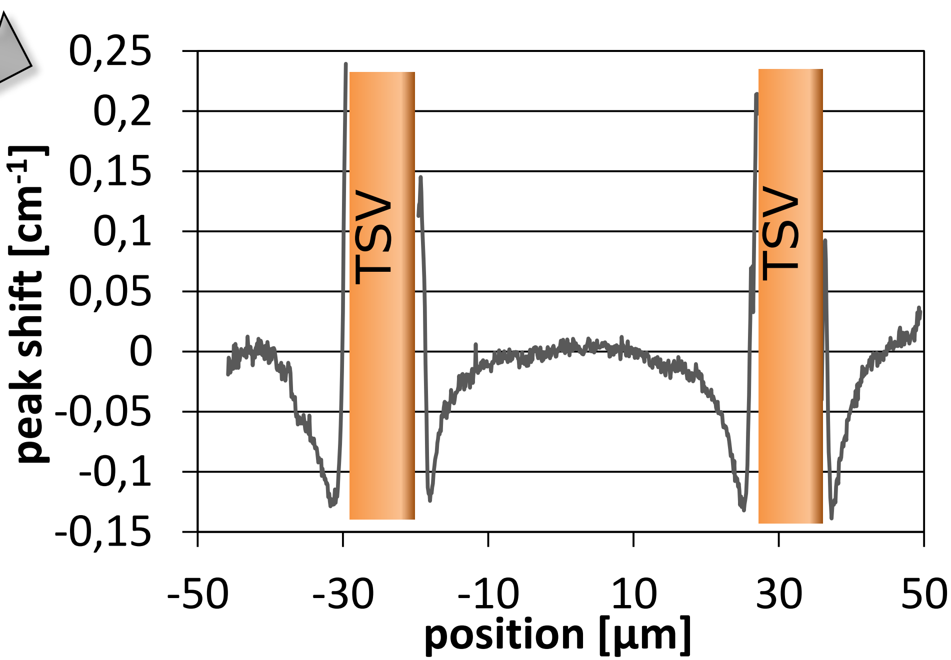
$$\begin{vmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) - \lambda & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{33} + \varepsilon_{11}) - \lambda & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) - \lambda \end{vmatrix} = 0 \qquad \Delta\omega = \omega - \omega_0 = \frac{\lambda}{2 \cdot \omega_0}$$

[de Wolf., Semicond. Sci. Technol. 11 (1996)]

- µRS measurement:



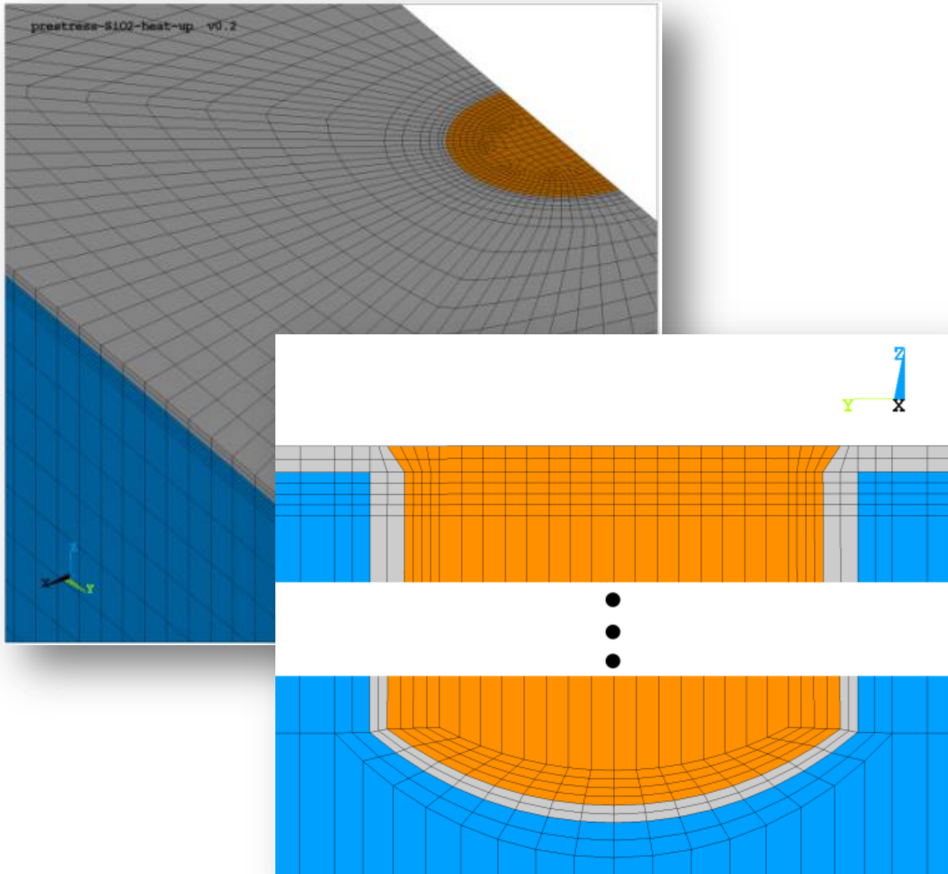
- line scans on the substrate surface over TSVs
- step size 100 nm
- laser wavelength 442 nm
- spot size 1 µm
- penetration depth 240 nm



→ stresses near the TSV interface

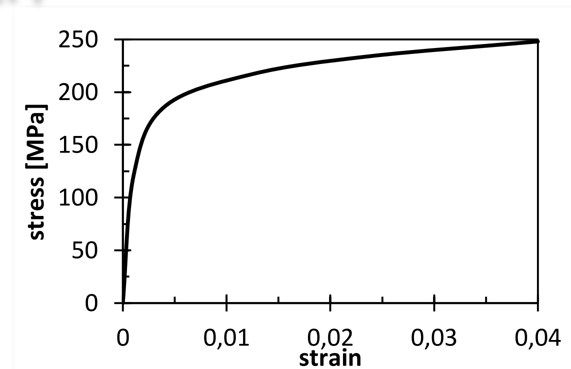
→ tension fades with increasing distance to the TSV

- model details:



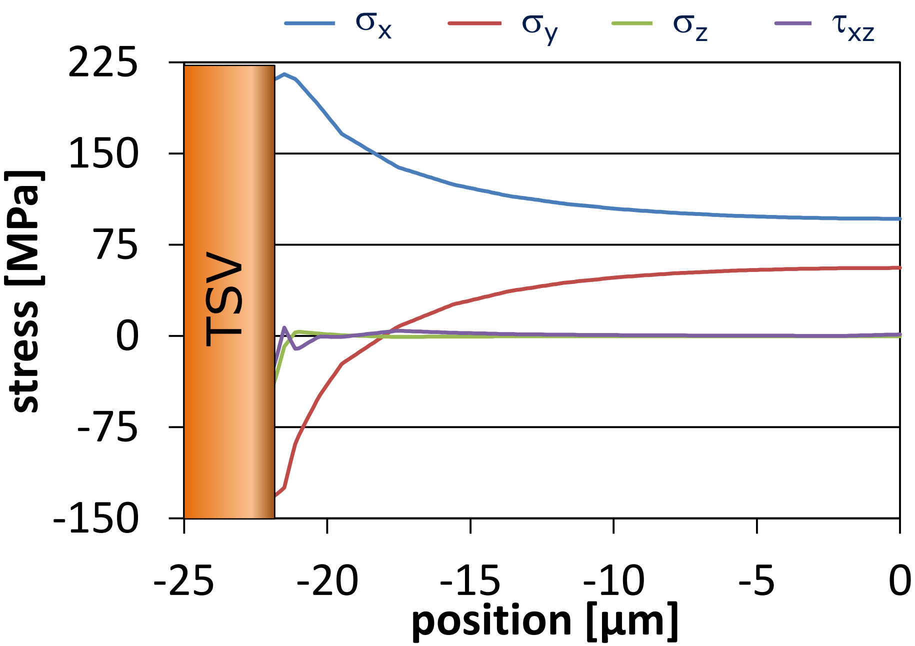
material	Cu	SiO_2	Si [100]
deposition	ECD	TEOS	-
Young's modulus [GPa]	121	71.4	168
TCE [10-6/K]	-380	240	-60
Poisson ratio [-]	0.3	0.16	0.22
CTE $[10^{-6}/K]$	17.3	0.5	2.8
modeling	elastic-plastic	elastic	elastic

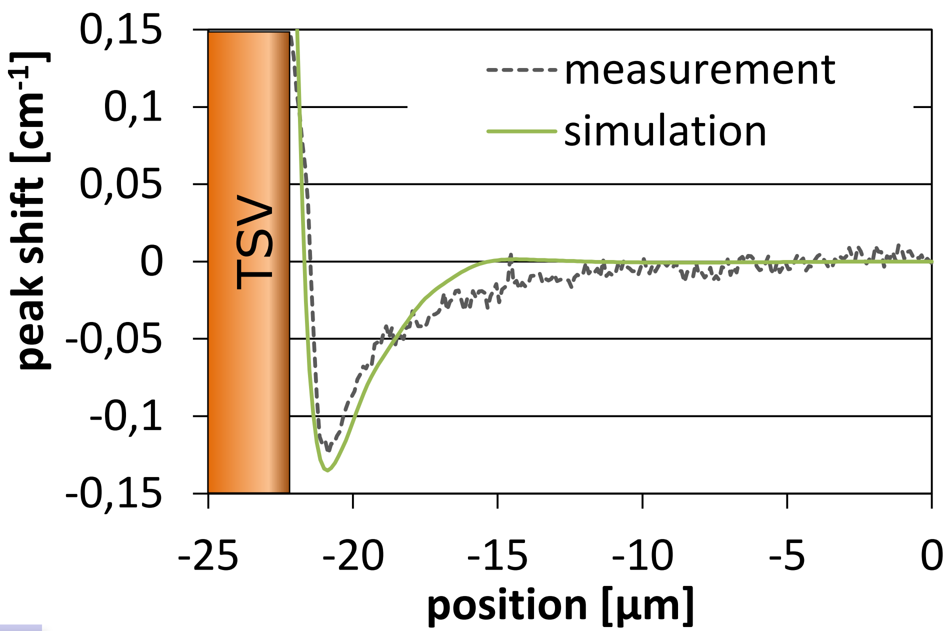
copper:



- stress free at 250 °C
- thermal load: cool down to room temperature

- results of simulation and measurement:





→ copper material behavior with strong influence on the stress state near the Cu-SiO_2-Si interface

→ SiO_2 layer on top of Si with relevant influence on the stress state in the center between the TSVs

→ evaluation routine delivers good approximations of the emerging stresses

Conclusions

- annealing at 250 °C for 2h increases warpage and copper protrusion associated with changes in copper crystal structure

→ copper protrusion emerges as a stress relief above recrystallization temperature and as consequence of coppers annealing behavior

→ annealing achieves the decrease of crystallographic defects

→ annealing causes additional mechanical stress

- Raman spectroscopy + FEM confirm warpage and protrusion measurements

→ stress distribution in silicon is complex

→ taking the right boundary conditions into account delivers a good match of simulation and measurement

Thanks for your attention!