EMC-Aware System Design - A focus on Integrated Circuits

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Airplanes

Rugby

Studying

Toulouse - the best place to be a student in France
CONTENTS

• General context
• Integrated Circuits
• Electromagnetic Compatibility
• Design Guidelines
1 GENERAL TRENDS
THE ELECTRONIC MARKET GROWTH

Adapted from Electronique International Mai 21, 2009
VISION 2020

• Increasing disposable income,

• Expanding urban population,

• Growing internet penetration and

• Availability of strong distribution network

MARKET GROWTH

Share of system sales
2020 vs 2015

Smartphones

Automotive

Internet of Things

PC

TV

Servers

Medical

Tablets

Game consoles

Growth

Electronic Market Growth
MOBILE BUSINESS

https://www.gsmaintelligence.com/

GLOBAL DATA

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>8,372,794,953</td>
<td>5,082,304,193</td>
<td>$1.06T</td>
<td>$10.25</td>
</tr>
</tbody>
</table>

Source: GSMA Intelligence 2017, current year-end data except interpolated subscribers and connections

Mobile subscriptions by technology (billion)

- 2G
- 3G
- 4G
- 5G
- LTE/WCDMA/GSM and LTE/CDMA
- WCDMA/GSM
- GSM/EDGE-only
- TD-SCDMA/GSM
- CDMA-only
- Other

3.7 billion LTE subscriptions by the end of 2020

http://www.ericsson.com/ericsson-mobility-report
• Growth in 2016 was **stalling** (+5% smartphones)
• Consumer demand was **sluggish** (tablets, laptops).
• Demand for **Internet of Things (IoT)** wasn't growing fast enough to offset declines
• **Price, security and ease-of-use** remain barriers to the adoption of new IoT devices and services.
TOWARDS AUTOMATIC DRIVE

• 2020: Injury-free driving
• 2030: Accident-free driving?
• 2040: Autonomous driving?
2 TECHNOLOGY TRENDS
SCALE DOWN BENEFITS

- Smaller
- Faster
- Less power consumption
- Cheaper (if you fabricate millions)
- Room for other devices

Power

- 65nm
- 28nm
- 14nm

-50%
-80%
<table>
<thead>
<tr>
<th>Technology</th>
<th>130nm</th>
<th>90nm</th>
<th>45nm</th>
<th>28nm</th>
<th>14nm</th>
<th>5nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complexity</td>
<td>100M</td>
<td>250M</td>
<td>500M</td>
<td>2G</td>
<td>7G</td>
<td>150G</td>
</tr>
<tr>
<td>Packaging</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mobile generation</td>
<td>3G</td>
<td>3G+</td>
<td>4G</td>
<td>4G+</td>
<td>5G</td>
<td>2020</td>
</tr>
<tr>
<td>Embedded blocks</td>
<td>Core+ DSP 1 Mb Mem</td>
<td>Core DSPs 10 Mb Mem</td>
<td>Dual core Dual DSP RF Graphic Process. 100 Mb Mem Sensors</td>
<td>Quad Core Quad DSP 3D Image Proc Crypto processor Reconf FPGA, Multi RF 1 Gb Memories Multi-sensors</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Mobile Communications**

- **2004**: 130nm, Core+ DSP, 1 Mb Mem
- **2007**: 90nm, Core DSPs, 10 Mb Mem
- **2010**: 45nm, Dual core Dual DSP, RF Graphic Process. 100 Mb Mem Sensors
- **2013**: 28nm, Quad Core Quad DSP, 3D Image Proc, Crypto processor, Reconf FPGA, Multi RF, 1 Gb Memories, Multi-sensors
- **2016**: 14nm
- **2020**: 5nm

-**Mobile generations**

- 3G
- 3G+
- 4G
- 4G+
- 5G

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**Department of Computer & Electrical Engineering**

**Université de Toulouse**
GOING ATOMIC SCALE

- 14-nm Xeon by Intel™
- IBM, GlobalFoundries, Samsung, SUNY first 7-nm testchip 2017
- Qualcomm™ Snapdragon X50

Si lattice: 0.23 nm
Stacked process layers

- 8, 16, 32 layers of active devices
- 1 tera-bit/cm² achieved 5 years ahead from roadmaps
High Bandwidth Memory (HBM) Hybrid Memory Cube (HMC)

<table>
<thead>
<tr>
<th></th>
<th>HBM2</th>
<th>HMC Gen3</th>
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</thead>
<tbody>
<tr>
<td>Density</td>
<td>8 GB (4GB)</td>
<td>8 GB (4GB)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>256 GB/s</td>
<td>480 GB/s (320 GB/s)</td>
</tr>
<tr>
<td>IO</td>
<td>Parallel (1G – 2G), 8 channels, 128b per channel</td>
<td>SerDes (up to 30G), 4(2) links per HMC, 16 lanes/link</td>
</tr>
<tr>
<td>Package Type</td>
<td>Si-interposer</td>
<td>Discrete (SerDes)</td>
</tr>
<tr>
<td>Expansion Capability</td>
<td>No</td>
<td>Yes, via chaining</td>
</tr>
<tr>
<td>Memory Access</td>
<td>DDR</td>
<td>Packet based</td>
</tr>
<tr>
<td>Power</td>
<td>Lower</td>
<td>Higher</td>
</tr>
<tr>
<td>Memory Suppliers</td>
<td>SK Hynix and Samsung</td>
<td>Only Micron</td>
</tr>
<tr>
<td>Thermal Dissipation Req.</td>
<td>High (Logic + DRAM in single 2.5D ASIC package)</td>
<td>Lower (discrete ICs)</td>
</tr>
</tbody>
</table>

http://www.eejournal.com/article/20170102-hbm-hmc/
GOING 3D – Package on Package

E. Sicard, EMC performance analysis of a Processor/Memory System using PCB and Package-On-Package, EMC Compo 2015 Edinburgh
THERE IS PLENTY OF SPACE ON THE TOP

- 3D technology uses stacked dies, through-silicon-vias
- Enables 10-20 Gb/s/pin at 1.0V
- Samsung 3D (Galaxy 6) vs PoP (Galaxy 5):
  - 30% faster
  - 20% less power
  - Less heat

http://www.youtube.com/watch?v=Rw9fpsigCfk
3

ELECTROMAGNETIC COMPATIBILITY
ONE ACRONYM – TWO PROBLEMS

- **SUSCEPTIBILITY TO INTERFERENCE**
  - Radar
  - Equipment
  - Boards
  - Components

- **EMISSION OF PARASITIC NOISE**
  - Personal Devices
  - Interferences
  - Safety systems

- Hardware fault
  - Software failure
  - Function Loss
SUPPLY VOLTAGE SCALE DOWN

- Less noise margin (<100 mV in 7-nm)

Supply (V)

Technology node

0.35µ  0.18µ  130n  90n  65n  45n  32n  20n  14n  10n  7n

0.7 V inside, 1.2V outside

I/O supply

Core supply

SIITME

10-nm technology
2, 3, 4, 5G mobile frequencies

**Today**
- 4G 800
- 2-3G 900
- 2-4G 1800
- 3G 1900
- 4G 2600

**Tomorrow**
- 5G 700
- 5G 3300
- 5G 4400
- 5G 26 250
- 5G 42 500
I/O Technology

- Multi-Giga-Bit link between processors & memories: video, object recogn., 3D capture
- Generation 4x and 5 on the market
- Generation 6 under development

Data Rate per pin (Gb/s)

100 Gb/s

10 Gb/s

1 Gb/s

DDDR4x: 230 ps, 0.25 V swing

Graphics trends

Low power trends

DDR trends

SIITME
Technology

- Nano-CMOS operates below 1V, noise margin around 50 mV
- Close to medium voltage (12, 24, 48 V) and high voltage (98, 240, 300, 400, 850 V) functions
- ADC with 16-24 bit resolution work at 10-100 μV resolution
4

DESIGN GUIDELINES
• Use tools, guidelines and trainings in EMC of Integrated circuits, for improved EMC before fabrication
• Place supply pairs close to noisy blocks
• Place enough supply pairs: Use One pair (VDD/VSS) for 10 IOs

9 I/O ports
• Reduce current loops that provoke magnetic field

Added contributions

EM wave

current

Lead

Die

current

Lead

Radiated field

Reduced contributions

EM wave

Reduced contributions

Currents

Reduced field
DESIGN GUIDELINES – REDUCE SWITCHING NOISE

- Reduction of clock buffer’s drive
- Spread of the switching
- 20dB noise reduction

- Reduce drive, limit slew rate,
- Adapt impedance,
- Add local decoupling
- 20dB noise reduction

DESIGN GUIDELINES – ISOLATE AND DECOUPLE

- On-chip decoupling
- Resistive supply path
- Substrate isolation
- Separate supply
- Separation between incompatible blocks

Immunity level (dBm)

No rules to reduce susceptibility

Substrate isolation

Decoupling capacitance

Frequency / MHz

Susceptibility / dBm

Work done at Eseo France (Ali ALAELDINE)
• Graphene in stacked dies
• 10-15dB coupling reduction

DESIGN GUIDELINES - SHIELDING

• Thin magnetic-nonmagnetic multi-layered structure
• Trench-via array and multi-layered conductor structures (5G, 28-39 GHz)

CONCLUSION
• The electronic market growth should be driven by 5G mobile, automatic drive, Internet of Things, etc.
• The trends towards nano-CMOS have been illustrated
• EMC concerns in terms of noise margin, higher frequencies and IO bandwidth
• Design guidelines for improved EMC have been introduced
Thank you for your attention

Special thanks to Prof. Norocel CODREANU, CETTI