Through Silicon Vias Annealing: A thermo-mechanical assessment

P. Saettler\(^{(1)}\), K. J. Wolter\(^{(1)}\), M. Hecker\(^{(2)}\), M. Boettcher\(^{(3)}\) and C. Rudolph\(^{(3)}\)

\(^{(1)}\) Technische Universität Dresden, Electronics Packaging Laboratory
\(^{(2)}\) Globalfoundries Dresden Module One LLC & Co. KG
\(^{(3)}\) Fraunhofer IZM-ASSID

Bucuresti, October 24\(^{th}\) 2014
- **Introduction:**
  - 2,5 and 3D Integration

- **Motivation:**
  - TSV annealing aspects

- **Annealing characterization:**
  - die warpage
  - copper protrusion
  - EBSD on TSVs

- **FEM and μ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results

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**3D architecture including TSVs**

- Sn
- Cu
- Ti - barrier
- Cu - ECD
- Si - substrate
- SiO₂ - CVD TEOS - Isolation
- Cu₃Sn
Introduction: Package on Package

Source: Yole 2012
### Introduction: 2.5D vs. 3D-Integration

<table>
<thead>
<tr>
<th></th>
<th>several standard packages</th>
<th>2.5D SiP</th>
<th>3D SiP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology and infrastructure maturity</td>
<td>+</td>
<td>-</td>
<td>--</td>
</tr>
<tr>
<td>Electrical bandwidth</td>
<td>-</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>Power consumption</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Heterogeneous integration</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Size</td>
<td>-</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>Thermal Management</td>
<td>++</td>
<td>+</td>
<td>-</td>
</tr>
</tbody>
</table>

Source: Yole 2012
Introduction: 2.5D Integration

TSV-Annealing: A thermo-mechanical assessment

Source: Yole 2012
Introduction: 2,5D und 3D Integration

source: Yole Polymeric materials 2012
Introduction: TSV - dimensions

Typical diameters: 5-20 µm
Aspect ratio: up to 1:10
Isolation (SiO₂) 400 nm
Barrier-Layer (Ta/TaN) respectively 80 nm
Seed-Layer (Cu) 600 nm

Etched Si (Bosch process)
Scallops in Si and SiO₂ isolation layer
unfilled TSVs (d=5µm)
Cu-filled TSVs (d=20µm)

[Wolf et al., ESTC, 2010]
[Powel et al., IITC, 2008]
[Laviron et al., ECTC, 2009]
[Wolf et al., ESTC, 2010]
Moore’s Law vs. More-Than-Moore

Moore’s Law

2D SoC

Long Wiring (from A to B) in 2D SoC

For both cases, Thermal Management is a big issue!

More-than-Moore

3D IC Integration

Short Wiring (from A to B) in 3D IC Integration with TSVs, thin chips, and microbumps,

3D Si Integration

Thin Chips

Wafer-to-wafer bonding

Very short wiring in 3D Si integration with very tiny TSVs, thin wafers/chips, and bumpless (no bumps!)

Thermal management is a huge problem

TSV-Annealing:
A thermo-mechanical assessment

[Lau, ECTC, 2010]
Introduction: Via-technologies

TSV-Annealing:
A thermo-mechanical assessment

Source: Yole 2012

- a) Via first
  TSV->Thinning-> CMOS

- b) Via middle
  CMOS->TSV->Thinning

- c) Via last
  CMOS->Thinning->TSV
- **Motivation:**
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- **Annealing characterization:**
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  - EBSD on TSVs

- **FEM and µ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results

3D architecture including TSVs

Sn
Cu
Ti - barrier
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Si - substrate
SiO₂ - CVD TEOS - Isolation
Cu₃Sn
Motivation: Copper Protrusion

- layer cracking and delaminations due to copper protrusion

[w/o annealing] (a) [annealing (0.5h/450°C)] (b)

Motivation: Copper Protrusion

TSV-Annealing: A thermo-mechanical assessment

[Lu et. al., Thermo-mechanical Reliability Challenges of 3D Interconnects]

[Lin et. al., IEDM 2010]
Motivation: stresses caused by TSV fabrication

- die/wafer warpage
- degradation of device performance
- Si substrate cracking

TSVs:
- Ø = 5 µm
- depth = 120 µm
- pitch = 10 µm

How to characterize and calculate stresses in silicon?!
TSV-Annealing: A thermo-mechanical assessment

Electronics Packaging Laboratory

TSV-structure is on minimum stress at annealing temperature.

Hypothesis: Annealing behavior of Copper

unstable material behavior

crystalllographic defects and residual stresses

decrease of grain growth

unstable material behavior

crystalllographic defects and residual stresses

decrease of grain growth

Tensile Strength Residual Stress

Hardness Recovery

Recrystallization Grain Growth

26.10.2014 slide 13

Materials Science for Engineering Students; Traugott Fischer; 2009
Werkstoffkunde für Ingenieure; Eberhard Roos; 2008
proof of hypothesis by experiment and simulation

- perform annealing with supplementary characterization
- search for increased warpage, protrusion and grain growth indicating coppers annealing behavior
- measure stresses using Raman spectroscopy
- implement simulation model using hypothesis assumptions
- stress free at annealing temperature
- cool down to room temperature as thermal load

compare measured and calculated stresses
- **Annealing characterization:**
  - die warpage
  - copper protrusion
  - EBSD on TSVs
- **FEM and µ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results
Experimental: Test samples

- **die samples:**
  - 3 cm x 3 cm x 700 µm
  - samples taken after copper fill and overburden CMP (unthinned die)
  - 600 nm SiO$_2$ on top
  - TSV-pitch 55 µm

- **experimental:**
  - annealing conditions:
    - T: 250 °C
    - t: 2 h

- **measurement:**
  - warpage
  - grain structure
  - copper protrusion
  - µRS
Experimental: Die Warpage

- measurement of die warpage:

- confocal sensor
- creation of height maps
- evaluation of diagonals bending radii

height map of the test die back sides

- bending even without annealing
- increased warpage after annealing (decreased bending radius)
- stress increase

Graph:
- w/o annealing
- 2h @ 250°C
- bending radius [m]
- 820 [µm]
- 810
- 800
- 790
- 780
- 780

- 250,00
- 200,00
- 150,00
- 100,00
- 50,00
- 0,00

- w/o annealing
- after annealing
Experimental: Copper Protrusion

- measurement of copper protrusion:
  - confocal microscopy
  - creation of height maps
  - evaluation of TSV profiles average heights

- height map of a TSV's copper protrusion

- height profile and measured copper protrusion

→ copper protrusion: 61 ± 4 nm in average
**Electron BackScatter Diffraaktion – experimental arrangement and functional principle:**

- Sample with an angle of 70° inside the SEM
- Incident electron beam scatters inelastic on lattice atoms
- Bragg conditions → constructive interference (diffraction pattern – Kikuchi-pattern)
- CCD camera records pattern from phosphorus screen
- comparison of grain structures after 4 h annealing:

Annealing above recrystallization temperature creates grain growth.
- comparison of grain size distributions:

- initiated grain growth
- only marginal grain size changes measured → additional evaluation of twin boundaries as crystallographic defects
Evolution of crystal structure as result of annealing

- **Misorientations between grains / twin boundaries:**
  - CSL – coincident site lattice
  - CSL boundary - some of the atoms in two crystal lattices separated by the boundary are coincident
  - typical twin boundaries of copper:

<table>
<thead>
<tr>
<th>Σ Type</th>
<th>Angle</th>
<th>Axis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Σ3</td>
<td>60°</td>
<td>111</td>
</tr>
<tr>
<td>Σ9</td>
<td>38.94°</td>
<td>110</td>
</tr>
<tr>
<td>Σ27a</td>
<td>31.59°</td>
<td>110</td>
</tr>
<tr>
<td>Σ27b</td>
<td>35.43°</td>
<td>210</td>
</tr>
</tbody>
</table>

[www.hkitechnology.com]
Evolution of crystal structure as result of annealing

- Misorientations between grains / twin boundaries:

<table>
<thead>
<tr>
<th>CSL</th>
<th>w/o annealing</th>
<th>2h @ 250°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Σ</td>
<td>Length [µm]</td>
<td>Length [µm]</td>
</tr>
<tr>
<td>3</td>
<td>2230±52</td>
<td>1427±63</td>
</tr>
<tr>
<td>9</td>
<td>233±9</td>
<td>153±7</td>
</tr>
<tr>
<td>27a</td>
<td>37±1</td>
<td>26±2</td>
</tr>
<tr>
<td>27b</td>
<td>51±3</td>
<td>20±2</td>
</tr>
</tbody>
</table>

- Decreased crystallographic defects due to annealing
- **FEM and μ-Raman spectroscopy:**
  - Raman measurement
  - validation of FE-results

3D architecture including TSVs
Raman spectroscopy for stress measurement:

- strains effect Raman peaks
- uniaxial stress model:
  - positive shift - compression
  - negative shift - tension
- **BUT**: peak position is dependent on all strain tensor elements
- general stress calculation rule needed

conversion of strains into Raman Shifts:

\[
\begin{vmatrix}
    p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) - \lambda & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\
    2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{33} + \varepsilon_{11}) - \lambda & 2r\varepsilon_{23} \\
    2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) - \lambda
\end{vmatrix} = 0
\]

\[
\Delta\omega = \omega - \omega_0 = \frac{\lambda}{2\cdot\omega_0}
\]

- **μRS measurement:**

  - line scans on the substrate surface over TSVs
  - step size 100 nm
  - laser wavelength 442 nm
  - spot size 1 µm
  - penetration depth 240 nm

  - stresses near the TSV interface
  - tension fades with increasing distance to the TSV

  - peak shift [cm\(^{-1}\)]
  - position [µm]

  ![Graph showing peak shift and position](image-url)
- model details:

- stress free at 250 °C
- thermal load: cool down to room temperature

### Material Properties

<table>
<thead>
<tr>
<th>material</th>
<th>Cu</th>
<th>SiO₂</th>
<th>Si [100]</th>
</tr>
</thead>
<tbody>
<tr>
<td>deposition</td>
<td>ECD</td>
<td>TEOS</td>
<td>-</td>
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<tr>
<td>Young’s modulus [GPa]</td>
<td>121</td>
<td>71.4</td>
<td>168</td>
</tr>
<tr>
<td>TCE [10⁻⁶/K]</td>
<td>-380</td>
<td>240</td>
<td>-60</td>
</tr>
<tr>
<td>Poisson ratio [-]</td>
<td>0.3</td>
<td>0.16</td>
<td>0.22</td>
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<tr>
<td>CTE [10⁻⁶/K]</td>
<td>17.3</td>
<td>0.5</td>
<td>2.8</td>
</tr>
<tr>
<td>modeling</td>
<td>elastic-plastic</td>
<td>elastic</td>
<td>elastic</td>
</tr>
</tbody>
</table>

### Copper

- Stress free at 250 °C
- Thermal load: cool down to room temperature
- results of simulation and measurement:

- copper material behavior with strong influence on the stress state near the Cu-SiO₂-Si interface
- SiO₂ layer on top of Si with relevant influence on the stress state in the center between the TSVs
- evaluation routine delivers good approximations of the emerging stresses
• annealing at 250 °C for 2h increases warpage and copper protrusion associated with changes in copper crystal structure

→ copper protrusion emerges as a stress relief above recrystallization temperature and as consequence of coppers annealing behavior

→ annealing achieves the decrease of crystallographic defects

→ annealing causes additional mechanical stress

• Raman spectroscopy + FEM confirm warpage and protrusion measurements

→ stress distribution in silicon is complex

→ taking the right boundary conditions into account delivers a good match of simulation and measurement
Thanks for your attention!